Analysis of HVDC Convertor Transformer Core Saturation Instability, and Design of a Data Acquisition System for its Assessment

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Abstract

This thesis is divided into two parts; The analysis of HVDC convertor transformer core saturation instability, and the design of a flexible data acquisition system for its assessment.

A linearised direct frequency domain analysis of the mechanism behind the core saturation instability is presented. Using linearised convertor transfer functions and transformer saturation characteristics on ac and dc equivalents, the system equations are solved to describe the phenomenon. A term, referred to as *Saturation Stability Factor*, is derived to measure the system susceptibility to such an instability.

The direct and quick solution of the method is used to reveal the characteristics of vulnerable systems. It is also used to determine effective and appropriate control measures. The predicted dynamics are validated with time domain simulations.

Harmonic instability problems with long time constants, such as core saturation instability, are suited to real time computer analysis. Such real time analysis requires a compatible data acquisition system to process and present the simulated data. The second part of this thesis describes the design of a powerful and yet flexible data acquisition system for these purposes.

A locally developed harmonic monitor, called CHART (Continuous Harmonic Analysis in Real Time) possesses several unique qualities, distinguishing it from other commercial systems. This thesis details the third generation of this system, known as CHART III, and its software architecture, referred to as the CHART III Virtual Operating System, which has transformed the dedicated harmonic monitor to a flexible multipurpose data acquisition system. The capability provided in the system is illustrated by several recent field measurements.

The understanding resulting from the theoretical analysis of the instability, and the development of CHART III, have paved the way for the real time analysis of the core saturation instability.

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Glossary

Abbreviations and Acronyms

A/D; ADC	Analog to Digital Convertor
ac	Alternating current
CADU	Control And Display Unit
CHART	Continuous Harmonic Analysis in Real Time
CIGRE	Conference Internationale de Grands Reseaux Electriques
CPU	Central Processing Unit
DAPM	Data Acquisition and Processing Module
dc	Direct current
DOS	Disk Operating System
DPR	Dual Port Random Access Memory
DSM	Digital Services Module
DSP	Digital Signal Processor
ESCR	Effective Short Circuit Ratio
Ethernet	A Standard 10 Mega bit per second local area network
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
GPIB	General Purpose Interface Bus
GPS	Global Positioning System
HVDC	High Voltage Direct Current
Internet	A global computer network protocol
iRMX	Intel Real Time Multitasking Operating System
iSBX	Intel System Bus eXtension
LAN	Local Area Network
MDI	Multiple Document Interface
MIX	Modular Interface eXtension
Multibus II	An advanced Intel multiprocessor bus architecture
NFS	Network File System

PC	Personal Computer
PI	Proportional/Integral
pps	Pulse per second
PPU	Parallel Processing Unit
PSB	Parallel System Bus
PSCAD/EMTDC	Electromagnetic Transient dc Simulation Program
RAM	Random Access Memory
RDCM	Remote Data Conversion Module
RS232; RS422	Serial communication protocols
RTC	Real Time Clock
RTDS	Real Time Digital Simulator
SBC	Single Board Computer
SCR	Short Circuit Ratio
SCSI	Small Computer Systems Interface
SRM	Sample Rate Multiplier
SSF	Saturation Stability Factor
TAXI	Transparent Asynchronous Transmitter/Receiver Interface
TCP/IP	Transmission Control Protocol / Internet Protocol
TMS320C31	A Texas Instruments 32 bit floating point digital signal processor
WAN	Wide Area Network
XDR	eXternal Data Representation

Chapter 1

Introduction

1.1 HVDC systems

Since the first commercial scheme in 1954, the HVDC technology has advanced at an unprecedented rate with currently, over 50 installations worldwide, and more schemes are expected in the future. This rapid growth of the HVDC industry is largely due to the astonishing development of the solid state HVDC convertor. The solid state thyristor is not only cheaper to manufacture and operate, but the improved technical performance over its mercury-arc predecessor has seen the take-over of the earlier schemes by thyristor technology.

The traditional economic advantage of HVDC transmission over long distances is still unchallenged by its AC counterpart, particularly those involving cable transmission. Its main drawback has been the high cost of the convertor stations, but advances in the solid state technology have reduced the cost for it to become economically viable over shorter distances. This is reflected by a growing number of back-to-back interties being used to interconnect ac networks. The better and faster controllability lends itself to the interconnection of large ac networks, and it is the more practical way for interconnecting ac systems of different frequencies.

One of the major appeals of HVDC schemes is their extremely high reliability. Most of the lengthy outages of HVDC schemes are not caused by failures in the convertor, but are due to failure of other ac components such as the convertor transformers or harmonic filters. Despite the many years of operation, the mercury-arc valves are still very reliable provided a high level of regular maintenance is being performed on the valves and the auxiliary equipment. The recently upgraded New Zealand HVDC link has opted to keep the mercury-arc valves, primarily due to economic reasons, and operates them alongside the new thyristor valves [O'Brien *et al.*, 1993]. The thyristor convertor has eliminated the problem of arc-backs and the built-in redundancy of the thyristor valves has greatly reduced the number of outages of the HVDC transmission system.

The growing experience with the HVDC technology, initially with the mercury-arc valves, and more recently with the thyristor valves, has helped to refine the technology and reduce the cost of such a system. Such high cost and technically intensive schemes, which were only seen in highly developed nations several years ago, have been taken up by the developing countries, with several schemes being planned in the Asia Pacific region alone. With the worldwide growing demand for electrical energy, the constantly improving cost and technical advantages of HVDC technology has firmly cemented its future in modern electrical power systems.

1.2 Computer analysis of power systems in real time

The advancement of computer technology has paved the way for the development of computer analysis of power systems. There is a wide range of computer analysis tools available, ranging from the traditional load flow programs to specialised algorithms for the analysis of harmonic interactions around the HVDC convertor. The use of better and more efficient problem solving methods has raised the understanding of the power systems and helps to maintain a more reliable and economic supply of electrical power.

Despite the vast capability of present day computers and the availability of various analysis tools, some of the power systems problems still cannot be predicted by existing computer models. These problems are generally discovered during or after commissioning, and therefore require additional time and investment to correct them. In each case, a thorough understanding of the problem is required to construct an accurate computer model for further studies.

One of the problems which is still eluding early detection through computer analysis is the harmonic instability caused by the HVDC convertor. Several types of harmonic instability have been identified including the convertor transformer core saturation instability, which involves an additional destabilising contribution caused by transformer saturation. It has been suggested that this type of instability is highly dependent on the operating conditions of the system [Ainsworth, 1977] and it is, therefore, difficult to pinpoint the cause of such an instability. Although HVDC hardware simulators have been widely used since the early days of HVDC technology, the difficulty of accommodating the necessary changes has prevented their use for studying this type of problem, leaving it to computer analysis.

The vast improvement in the computer processing capability has created a new approach to computer analysis which employs a parallel data processing architecture and enables computer simulation to be undertaken in real time. The Real Time Digital Simulator has already been used for testing relays and protection circuits, and can be an ideal tool for analysing power system problems with long time constants such as core saturation instability.

Power systems real time analysis requires that the simulated waveforms are processed and presented in real time. This calls for a data acquisition system capable of undertaking continuous real time measurements. Moreover, different problems usually have varying processing and presentation requirements, and therefore the data acquisition system has to possess sufficient flexibility to accommodate such customised uses.

1.3 Research objectives

The main motivation behind this project is to clarify the mechanism causing convertor transformer core saturation instability, and thus raise the level of understanding of the problem. A better comprehension of the problem may lend itself to more effective control solutions. With the help of a new convertor model in the frequency domain, Wood had initiated the analysis of this instability [Wood, 1993]. His work is extended in this thesis to incorporate and assess the effect of several practical aspects of the system into the studies.

Due to the long time constant associated with this type of instability, it is preferable to illustrate the instability using real time simulators. A corresponding data acquisition system would be needed, not only for demonstrating the mechanism of the instability, but also to implement appropriate detection and control measures.

Hence, the other objective of this project is to take advantage of the continuous real time data processing capability of a data acquisition system called CHART to study this instability. Continuous data processing ability is essential for the detection of any instability problem, such as the core saturation instability, which only occurs under certain operating conditions. The previous version of CHART was oriented primarily for harmonic measurements and no provision was made for other functions. Therefore, the system had to be revised and, in particular, a new software architecture developed to turn the system into a flexible tool suitable for analysing any HVDC related instability phenomena.

With such objectives, the research effort has been divided between the analysis of the core saturation instability using the new frequency domain technique proposed by Wood, and the development of the new version of CHART. The ultimate objective is to apply the acquired knowledge about the instability to a real time simulator model, and then make use of the new CHART system to detect and control the development of the instability.

Unfortunately, the present unavailability of a real time simulator to represent the instability prevented the final objective from being achieved. Instead, a non real time computer simulation tool was used to illustrate and validate the analysis of core saturation instability. However, it was possible to continue the development of a new version of the CHART system to detect and control the instability, and this capability is demonstrated with two field measurements, both having very different data processing requirements.

1.4 Thesis outline

The thesis is divided into two main parts, reflecting the two aforementioned objectives of this research. The first part describes the analysis done on the convertor transformer core saturation instability, while the second part is concerned with the transformation of the CHART system from a dedicated harmonic measurement instrument to a flexible real time data acquisition system.

Chapter 2 introduces the convertor transformer core saturation instability, with a brief literature review and the various techniques available for analysing it. The research direction of this analysis is also presented in this chapter.

A linearised frequency domain analysis of the instability, continued from the work of Wood, is described in Chapter 3. The derivation of a measure of system stability called the *Saturation Stability Factor* is explained. The predictions of system stability from the direct frequency domain approach are validated against time domain dynamic simulations.

Chapter 4 provides a comprehensive evaluation of the properties of HVDC systems which are prone to such an instability. The system characteristics considered are the system impedances, the convertor transformer magnetisation characteristics, the frequency response of the convertor controller and the steady state operating conditions of the convertor. The system stabilities at both the rectifier and invertor ends of a HVDC scheme are also discussed in this chapter. The likelihood of developing the instability in back-to-back interties is also investigated.

Chapter 5 is used to demonstrate the various control solutions for preventing the onset of core saturation instability. The parameters of the control solutions are obtained through the direct frequency domain approach of the *Saturation Stability Factor*.

In Chapter 6, the need of a flexible data acquisition system, for field measurements as well as for real time simulator studies, is discussed and the requirements of such a flexible system are outlined.

Chapters 7 and 8 describes the new version of a data acquisition system, known as CHART III. The hardware structure of the system is covered in Chapter 7, while Chapter 8 deals with the new software architecture. This new software architecture is regarded as the CHART III Virtual Operating System due to its resemblance to a typical computer operating system.

The flexibility provided in CHART III is demonstrated with two field measurements, described in Chapter 9 with a selection of field data acquired in the tests.

Finally, Chapter 10 concludes the research effort described in this thesis and discusses possible future works in both the analysis of core saturation instability, and the development and application of the CHART system.

Chapter 2

Convertor Transformer Core Saturation Instability

2.1 Introduction

HVDC systems with low short circuit ratios (SCR) have been known to experience problems of instability. This instability may be in the form of voltage fluctuation, frequency fluctuation or waveform distortion. The low SCR indicates high ac system impedance, whose high inductance may resonate with the reactive compensation capacitors and the harmonic filters commonly found at the convertor terminals. These resonance frequencies can be low, possibly as low as the second harmonic frequency. The resonances can be excited under certain operating conditions or in the event of fault, and the small initial distortion may develop to an instability. Instability related to the interaction of harmonics (or any non-integer frequencies) has been customarily referred as harmonic instability.

The problem of harmonic instability is not new, with several cases being reported in the 1960's. Ainsworth was the first to identify a form of harmonic instability related to the individual valve firing control [Ainsworth, 1967]. He introduced the use of a phase locked oscillator system [Ainsworth, 1968] as the control solution which is universally followed in existing HVDC installations. Since then, a wide range of approaches have been developed to analyse the phenomenon of harmonic instability. [Wood, 1993] contains a comprehensive review of the analysis techniques and the assumptions made in these approaches. Different forms of harmonic instability have since been identified, such as complementary resonances, composite resonances, cross-modulation and transformer core saturation instability.

The convertor transformer core saturation instability is a type of harmonic instability involving an additional amplifying effect from transformer saturation. Similar to other types of harmonic instabilities, the phenomenon has in the past been discovered during or after initial testing of the HVDC scheme. In some cases, it was encountered after the system had been commissioned and occurred only under certain unfavourable conditions. These events are clearly undesirable and ideally, the problem should be detected in the early planning stage of the project. Early detection will enable counter measures to be designed into the scheme and avoid the high cost and time involved with any modification at a later date. Furthermore, most HVDC schemes will be upgraded at some stage of their career, and it has to be ensured that the instability is avoided after the changes.

There have been several incidences of core saturation instability reported in the literature. The first identified case is at Kingsnorth [Ainsworth, 1977]. Since then, there have been a handful of reports citing this instability, at Nelson River scheme [Chand *et al.*, 1987], Blackwater back-to-back intertie [Stemmler, 1987] and the Chateauguay scheme [Hammad, 1992].

Despite these incidences, very few analyses of this phenomenon exists and this may have led to some cases being misinterpreted as another type of harmonic instability or resonance.

Different approaches have in the past been utilised to analyse the core saturation instability problem at different installations. Despite the different techniques, the control solutions are very similar typically involving some sort of firing angle modulation and in some cases the installation of additional harmonic filters. However, there are no cohesive indications among the studies to pinpoint the likelihood of a HVDC scheme experiencing such an instability. To carry out such predictions requires a thorough understanding of the mechanism behind the instability. A convenient approach able to provide an overview of the instability is also required. The objective of this research is to generate further knowledge about the phenomenon and use the knowledge to foresee the system susceptibility to this type of instability. Moreover, a better comprehension of the problem should lead to more effective solutions.

2.2 Historical review

Convertor transformer core saturation instability was first identified in the Kingsnorth HVDC scheme in the 1970's. A report to the CIGRE Study Committee No.14 [Ainsworth, 1977], correctly described the mechanism behind the instability as caused by a combination of a weak ac system and a dc side resonance near the fundamental frequency. This instability was detected by chance when the 12^{th} harmonic components of the distorted transformer magnetising current was magnified by a parallel resonance which existed under certain conditions on the ac side, in between the resonances of the 11^{th} and 13^{th} harmonic filters. This disturbed the filter tuning detection circuits and the total filter currents per arm sometimes exceeded the filter rating, causing the protection to shut down the link. However, the low order harmonics related to the build up of the instability never exceeded a rather small amplitude and this problem may have remained unnoticed if the aforementioned resonance did not exist. They successfully corrected the problem by incorporating an extra control loop to modulate the convertor firing angle according to the level of transformer saturation.

In 1980, an iterative technique was used to reanalyse this problem at the Kingsnorth scheme [Yacamini *et al.*, 1980b]. They demonstrated that this form of instability could only be shown with finite ac and dc side impedances. Based on iterative techniques described in earlier papers on convertor harmonic interaction [Yacamini *et al.*, 1980a] and transformer saturation [Yacamini *et al.*, 1978], they proposed that the instability was indicated when the iterative procedure failed to converge. Their findings have established the need for comprehensive calculations of the convertor harmonics under weak ac systems and with finite dc systems in order to analyse this phenomenon. The feedback effect of the convertor controller which can contribute to the magnification of the harmonics was also included in their model.

In 1987, Stemmler attempted an algebraic analysis on this subject. Using a steady state convertor transfer function, he analysed the core saturation instability detected at the Blackwater back to back intertie [Stemmler, 1987]. Neglecting the effect of commutation and firing angle control, he derived mathematical expressions to describe the harmonic voltages and currents on both sides of the convertor including the contribution from the transformer saturation. He reported a method of stabilisation by jointly modulating the firing angles at both the rectifier and invertor. The modulation made the convertor resemble a high inductance at the second harmonic on the ac side, preventing the distortion at this frequency from reaching the dc link. This particular paper demonstrated the benefits of using simplified algebraic analysis to gather insights into the problem which could lead to potential solutions.

Stemmler further demonstrates the viability of using the convertor controller to damp this phenomenon.

Hammad investigated the effectiveness of two measures undertaken at the Chateauguay scheme to overcome the 2nd harmonic problem [Hammad, 1992]. Using a combination of eigenvalue and frequency domain approach, he showed the destabilising effect of the TCR control at the 2nd harmonic resonance. However, it is unclear whether the development of this particular instability involves the saturation of the convertor transformer and therefore this instability may not be related to the core saturation instability. On the other hand, the highly destabilising effect of the TCR control might have overwhelmed the contribution from the transformer saturation. Nonetheless, he showed the viability of using an auxiliary dc control circuit to introduce external damping of the dc current at the fundamental frequency without affecting the original system natural modes of operation. It was also shown that the installation of tuned shunt capacitors at the Chateauguay scheme shifted the system resonance away from the 2nd harmonic, alleviating the second harmonic instability problem.

In 1994, Burton presented a time domain simulation based analysis of this instability [Burton, 1994]. Using a modified version of the 'HMAT' (Harmonic Matrix) method proposed by Larson to describe the ac-dc interactions [Larson *et al.*, 1989], he calculated the equivalent impedance of the convertor looking from either the convertor ac or dc terminal. The coefficients of the interaction matrix were determined from results of simulations. Fourier analysis was used to extract the magnitude and phase responses from the time domain waveforms. The equivalent convertor impedance was then combined with the ac or dc system impedance and the system is considered to be unstable if the real part of the resultant impedance is negative. He also used simulations and Fourier analysis to incorporate the effect of transformer saturation into the equations. Using a simplified HVDC system, he successfully demonstrated the development of this instability in the time domain.

In 1993, Wood developed a frequency domain transfer function technique to relate the noncharacteristic ac voltage and dc current to distortion in the convertor firing angle, ac side voltage and dc side current [Wood *et al.*, 1995a]. He applied this technique to introduce the concept of composite resonance at convertor station [Wood *et al.*, 1995b]. Based on some assumptions made by Stemmler, he incorporated a linear worst case scenario model of transformer saturation into his equations and proposed a term called *Saturation Stability Factor* (*SSF*) as a measure of the level of core saturation stability. Although he was able to verify the predictions for stable systems, he was unable to validate his prediction of instability with growing distortion in the time domain simulations. Nonetheless, his efforts laid the foundation for the research described in this thesis.

2.3 Analysis techniques

Numerous techniques have been developed over the years to analyse the interaction of noncharacteristic harmonic distortions around the HVDC convertor. Wood presented a comprehensive review of the methods used by various researchers to this date [Wood, 1993]. He summarises these techniques into three broad categories; the direct frequency domain approach, the iterative frequency domain approach and the numerical time domain approach.

The direct frequency domain approach assumes linear interactions between the harmonics around the convertor. The principle of superposition is often used to include the rest of the ac and dc networks into the model. This method has the advantage of low computational requirement and the ability to achieve quick solutions. However, the validity of the linear

approximation is the main issue that needs to be addressed when using this approach. Moreover, this approach usually results in a large number of individual terms generated, which often need to be neglected if it is to remain manageable.

In the iterative frequency domain technique, the switching of the convertor is usually simulated in the time domain while other interconnected components are described in their frequency domain equivalents. Numerical Fourier analysis and its inverse or any other frequency extracting methods are used to interface between the two domains. Recently, a new technique has been developed to simulate the convertor switching in the frequency domain and eliminates the need to digress into the time domain [Smith *et al.*, 1995]. Generally, the presence of instability is based on the non-convergence of the solution.

Thirdly, the numerical time domain approach particularly that based on the electromagnetic transient methodology, has been widely accepted as an accurate representation of the electrical power system. PSCAD/EMTDC [Woodford *et al.*, 1985] is one that has been optimised for use with HVDC system simulations. This technique was in the past used primarily for dynamic studies but with advances in computer technology, this method has been applied to analyse pseudo-steady state problems including the core saturation instability. However, it has been known to have difficulty in representing frequency dependencies. Furthermore, the long time constant associated with this instability makes this technique impractical unless some time-scaling procedures are used to speed up the simulations, as in [Burton, 1994].

Due to the complicated nature of the interaction of noncharacteristic harmonics around a convertor, the two latter numerical based techniques have gained favour with academics as well as in industry, ahead of the linear approximation approach. However, the ability of the direct frequency domain technique to provide wider insights into the mechanism of the interaction cannot be denied. This ability to paint a global picture of the interactions and the responses from various components fosters a better understanding of the phenomenon and should lead to more effective control solutions. Although numerical techniques allow complicated control strategies to be modeled in detail, they still require the use of a heuristic trial and error approach, coupled with experience and ingenious intuition to obtain the most appropriate solution.

Aside from the three aforementioned approaches, the analogue hardware simulator is another possibility. However, the difficulty and inflexibility of this method to accommodate changes in the analysed system tends to hamper its potential. Moreover, the accuracy of the scaled-down model, in particular the amount of damping provided by the components, needs to be validated against actual full size equipments.

Lastly, real time digital simulators exploit the parallel processing capability of today's computers to enable the computation of numerical time domain simulation in real time. It enjoys similar benefits but also suffers the same disadvantages as the numerical time domain technique except that it has overcome the problem of long simulation time. Provided the mathematical representations of the entities under analysis are accurate, this method is ideal for illustrating the build up of an instability in particularly those with long time constants such as the core saturation instability.

2.4 Research outline

Wood assumed a worst case scenario in his direct frequency domain analysis, which is impossible to replicate with existing simulation tools such as PSCAD/EMTDC which was

used by him to validate his model. This perhaps accounts for the difficulty encountered in his attempt to demonstrate the development of this instability by time domain simulation. This research extends his work by incorporating several factors which enable the analysis to deviate from the worst case scenario. These extensions enable a much fairer validation of the direct frequency domain technique against other approaches.

In this research, the frequency domain equivalent circuit developed by Wood is modified and used to establish wider insights into the mechanism of the instability. Linear approximation and the principle of superposition are used to simplify the HVDC convertor and its interconnecting networks into equivalent circuits suitable for evaluating the stability of the HVDC scheme. The harmonic contribution from the transformer saturation is also linearised and incorporated into the model. The outcome of the analysis is the modified *Saturation Stability Factor* (*SSF*) which indicates the susceptibility of a HVDC scheme to the instability.

With the long time constants involved, it would be ideal to verify the predictions made through the direct frequency domain approach with real time simulations. Systems such as the RTDS (Real Time Digital Simulator) [Rosendahl *et al.*, 1989] are ideal for studying this problem, provided a suitable data acquisition system can be found. The development of the CHART (Continuous Harmonic Analysis in Real Time) [Miller *et al.*, 1992] data acquisition system makes this approach feasible and worthwhile. However, the unavailability of the real time simulator to represent the instability prevents the employment of real time analysis of this instability in this research. Instead, the non-real time simulation package of PSCAD/EMTDC is used to validate the deductions made from the direct frequency domain approach. External disturbances are introduced into the simulations in order to speed up the build up of saturation in the transformer so as to reduce the simulation time.

The *SSF* approach provides us with the ability and opportunity to generate an overall picture of the instability phenomenon. With the capability of simple and quick solutions, it is used to investigate the characteristics of the instability and the properties of the HVDC schemes prone to such instability. The influence of the convertor controller and the effect of different modes of operation are also analysed with this method. Lastly, this direct frequency domain approach is used to illustrate several possible solutions to this instability problem.

The extended equivalent circuit is described in Chapter 3 which includes the convertor and transformer saturation models and the derivation and validation of the modified *Saturation Stability Factor* (*SSF*). The characteristics of HVDC systems prone to this instability are revealed using this technique and are presented in Chapter 4. Finally, Chapter 5 illustrates the use of this method to arrive at effective control solutions.

Chapter 3

Saturation Stability Factor

3.1 Introduction

This chapter details the derivation of the *Saturation Stability Factor* (*SSF*) as a measure of the level of system core saturation stability. It begins with the description of the harmonic interactions around the HVDC convertor with particular attention to the harmonic sequences related to this type of instability. This is followed by a brief introduction to the mechanism behind the instability. The chapter continues with the details of the two major components involved with the phenomenon, namely the HVDC convertor and the convertor transformer. The models are then used with ac and dc system equivalents to derive the *Saturation Stability Factor*. The analysis is tested on several systems and the results are verified by dynamic simulations.

3.2 HVDC-AC harmonic interactions

The subject of non-characteristic harmonic interactions around an HVDC convertor is not new, with the first published analysis undertaken in the late 60's [Ainsworth, 1967]. Since then, there have been a substantial number of publications on this issue and numerous techniques have been developed to analyse and describe such phenomena [Wood, 1993]. Figure 3-1 summarises the non-characteristic harmonic interactions between the ac side and dc side of the convertor. The presence of certain harmonic distortions on either side of the convertor will result in corresponding distortions on the opposite side. The presence of a harmonic distortion at k times fundamental frequency on the dc side of a 12-pulse HVDC

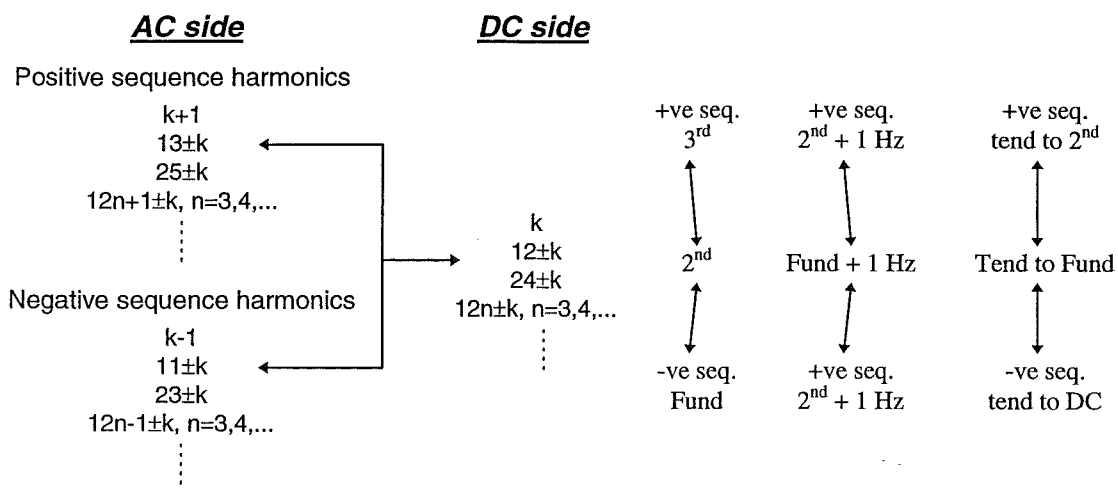

Figure 3-1: Harmonic interactions around HVDC convertor

convertor will produce on the ac side, positive sequence harmonics of orders k+1, 13±k, 25±k, 12n+1±k; n=3,4,..., and negative sequence harmonics of orders k-1, 11±k, 23±k, 12n-1±k; n=3,4,... These harmonic sequences are reflected back to the dc side as the k harmonic and various high orders harmonics of 12±k, 24±k, 12n±k; n=3,4,... Among these harmonics, the most significant terms are the first order components of k harmonic on the dc side, and the positive sequence k+1 and negative sequence k-1 harmonics on the ac side. The higher harmonics are an order of magnitude smaller than the lower order harmonics. Therefore, for most analyses, particularly those with small distortion levels, it is reasonable to ignore the contribution from high order harmonics.

With the high order harmonics ignored, the presence of a 2nd harmonic distortion on the dc side will result in a positive sequence 3rd harmonic and a negative sequence fundamental frequency component on the ac side. Equally, if there is a distortion near the fundamental frequency such as at 51Hz on the dc side, the distortions on the ac side would be near the second harmonic (101Hz) for the positive sequence component and near dc (1Hz) for the negative sequence component. As the frequency of the dc side distortion approaches fundamental frequency, the lower corresponding frequency component on the ac side, which is in the negative sequence format, will be approaching 0Hz, ie. approaching dc.

If the dc side distortion is exactly at fundamental frequency, the negative sequence component on the ac side is true dc, but with different levels in the three phases, which is customarily regarded as "unbalanced dc" generated by the convertor. However, the sum of the dc distortions in the three phases will be zero, and these distortions can in fact be written mathematically in a negative sequence format as follow,

$$\begin{aligned} I_a &= |I|\cos(0\cdot t+\delta+0^0) \\ I_b &= |I|\cos(0\cdot t+\delta+120^0) \\ I_c &= |I|\cos(0\cdot t+\delta+240^0) \end{aligned} \tag{3.1}$$

This form of distortion can be represented by three stationary vectors of similar length, and oriented in the negative sequence format as shown in Figure 3-2. This form of dc current

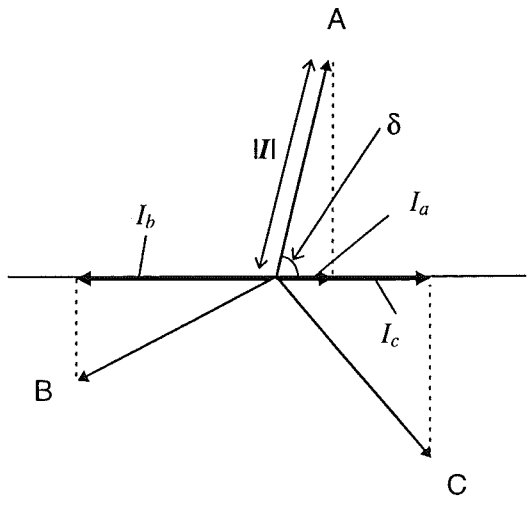

Figure 3-2: The form of negative sequence dc produced by HVDC convertor

generated by the convertor is arbitrary called "negative sequence dc current". This concept is best understood by considering a frequency close to fundamental on the convertor dc side, and letting it tends towards the fundamental frequency. The corresponding lower frequency component on the ac side will tend towards dc, but the combination of the three phases is still oriented in the negative sequence format.

The negative sequence dc concept is important in the analysis of convertor transformer core saturation instability because the distortion on the convertor dc side, related to this instability, is close to the fundamental frequency. Therefore, the more significant harmonic distortions on the convertor ac side concerning this instability are the positive sequence second harmonic and the negative sequence dc. The dc current will tend to saturate the transformer core which may ultimately lead to an instability.

3.3 Mechanism behind core saturation instability

The mechanism of the convertor transformer core saturation instability phenomenon can be demonstrated using the block diagram of Figure 3-3. If a small level of positive sequence second harmonic voltage distortion exists on the ac side of the convertor, a fundamental frequency distortion will appear on the dc side. Through the dc side impedance, a fundamental frequency current will flow, resulting in a positive sequence second harmonic current and a negative sequence dc current flowing on the ac side. The dc current flowing on the ac side will begin to saturate the convertor transformer, resulting in a multitude of harmonic currents being generated, including the positive sequence second harmonic current. Associated with this current will be an additional contribution to the positive sequence second harmonic voltage distortion and in this way the feedback loop is completed. The stability of the system is determined by the characteristics of this feedback loop.

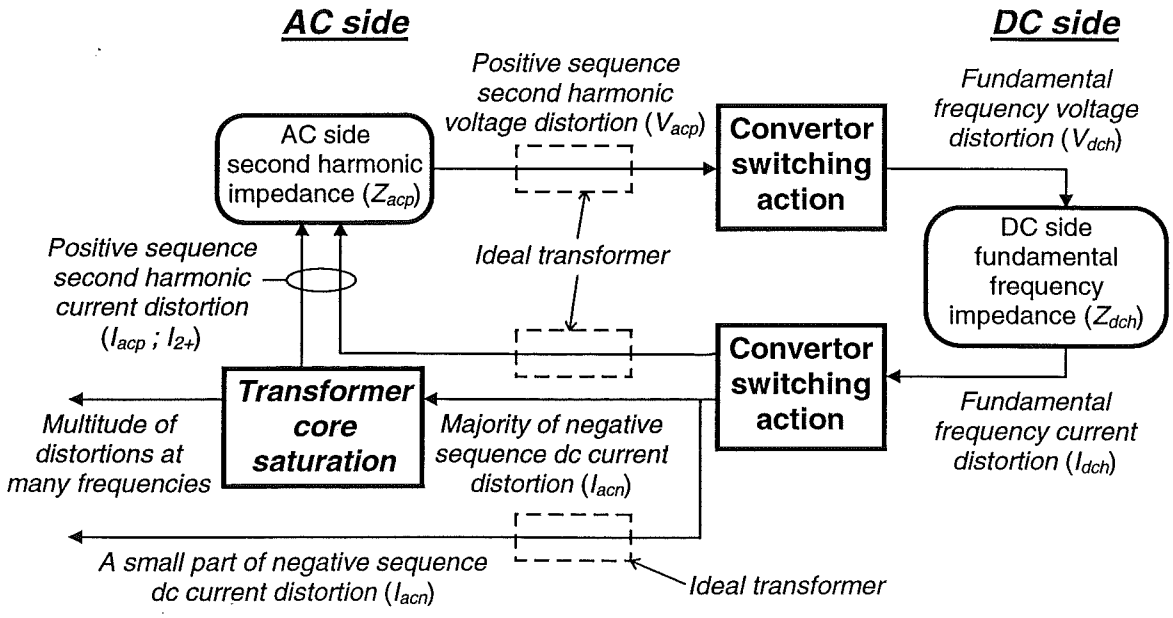

Figure 3-3: Mechanism of core saturation instability

In Figure 3-3, the aforementioned instability feedback loop does not involve the entirety of the negative sequence dc current produced by the convertor. This is because, in practice, the dc side distortion is never exactly at the fundamental frequency, and therefore, the negative

sequence dc is not a true dc but is varying slowly. This variation can be visualised by the slow rotation, in clockwise or anti-clockwise direction, of the dc vectors of Figure 3-2. The level of dc component in the transformer valve side current will be changing and is in fact transferring itself between phases in a cyclic manner. However, since the variation is near dc, the phrase "negative sequence dc" is used in this thesis to refer to this extremely slow varying distortion which is oriented in a negative sequence format as explained in the preceding section. This variation, although is sufficiently slow to cause transformer saturation, is also sufficiently fast for a percentage of it to pass through the transformer and into the ac system. The faster the variation of this negative sequence dc, the more of it will pass through the transformer and the less of it will saturate the transformer, and vice versa. The portion that passes through the convertor transformer may tend to dc-bias other transformers in the ac system, but it is unlikely to cause significant saturation to further contribute to the build-up of the instability.

The onset of core saturation instability is closely related to the saturation level of the convertor transformer. In this analysis, this instability is broadly divided into two categories, distinguished by their starting conditions. The first type has a spontaneous nature as it develops under normal operating condition without any external stimulus. System imbalances or asymmetry in the convertor firings will result in low level of transformer saturation which can ultimately develop into an instability. Study of this type of instability requires the evaluation of the transformer response at low saturation levels. The second type is referred as kicked-started instability which may see substantial transformer saturation as the starting condition. Some disturbances may impress high level of saturation on the convertor transformer and consequently result in the development of core saturation instability even after the disturbance. For this latter category of instability, the transformer response at high levels of saturation has to be determined.

To describe the characteristics of the instability feedback loop requires models of the convertor and the convertor transformer saturation. A linearised convertor model based on the work of Wood [Wood, 1993], [Wood *et al.*, 1995a], used to describe the transfer of harmonic sequences through the convertor is introduced in the next section. It is followed by the derivation of a simplified transformer saturation model accounting for the additional positive sequence second harmonic current distortion resulting from the saturation.

3.4 Convertor model

Wood represents the operation of the convertor in the frequency domain with a linearised transfer function describing the conduction and non-conduction periods of the thyristors. The transfer function is established by first defining the modulating function of an ideal convertor without any commutation period. The effect of the commutation period and its variation are derived separately and summed with the ideal function to build up the transfer function for a non-ideal convertor. The frequency spectrum of this transfer function is then derived to construct a convertor model in the frequency domain. This transfer function basically describes the transfer of ac side voltage distortions to the dc side and the dc side current distortion to the ac side. Intuitively, it also outlines the principle function of the convertor in converting the fundamental frequency voltage on the ac side to the intended dc voltage. The new model has been validated with dynamic simulations using PSCAD/EMTDC and close agreements were observed from the two approaches [Wood, 1993].

The convertor transfer function is a modulating function, but is also modulated by the variation in the firing angle, the ac voltage and the dc current. These variations can significantly affect the frequency spectrum of the transfer function and hence the transfer of

harmonics through the convertor. Using small signal analysis, Wood establishes the frequency spectrum of this modulated transfer function and uses it to describe the harmonic interactions around the convertor.

This model is not limited to characteristic frequencies or integer harmonics, and has shown that a single non-characteristic frequency results in a proliferation of frequencies on both sides of the convertor. However, taking only the most significant terms results in two components on the ac side separated by twice the fundamental frequency and one component on the dc side centred between the two ac side frequencies. The higher frequency on the ac side is of positive sequence while the lower frequency is of negative sequence. Figure 3-4 illustrates this harmonic interaction around a convertor. The voltage and current sources are respectively the voltage and current distortions at their corresponding frequencies if they exist in the system.

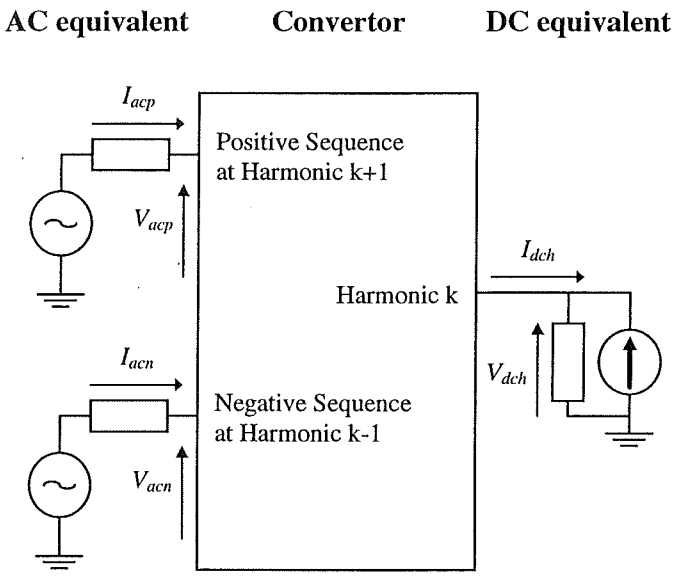

Figure 3-4: First order harmonic interactions around a convertor

From this figure, a set of simultaneous equations can be written to individually define the transfer from one distortion to another. By expressing these frequencies in vectorial form, the interaction between these most significant frequencies can be described with a 3x3 matrix of equation 3.2. The derivation of each of the elements within the matrix are detailed in [Wood, 1993] and is summarised in Appendix A.

$$\begin{bmatrix} V_{dch} \\ I_{acp} \\ I_{acn} \end{bmatrix} = \begin{bmatrix} a & b & c \\ d & e & f \\ g & h & i \end{bmatrix} \cdot \begin{bmatrix} V_{acp} \\ V_{acn} \\ I_{dch} \end{bmatrix} \tag{3.2}$$

Implicit in this expression is that the V_{acp} and I_{acp} are the higher frequency positive sequence components on the ac side at one harmonic higher than the dc side components of V_{dch} and I_{dch}, which are in turn one harmonic higher than the negative sequence components of V_{acn}

and I_{acn} on the ac side. In the analysis of core saturation instability, V_{acp} and I_{acp} are at the second harmonic, V_{dch} and I_{dch} at the fundamental frequency and V_{acn} and I_{acn} at dc[1].

The elements within the matrix are calculated from average values of the convertor operation in the steady state. The response of the convertor controller and the signal transducers are incorporated. The response of a constant current controller is included in elements c, f and i which accounts for the transfer to the three left hand side harmonics through the controller loop.

3.5 Transformer saturation model

It is evident that the onset of the core saturation instability is highly dependent on the effect of the transformer saturation. For the purpose of this analysis, the transformer saturation model concentrates on the amount of positive sequence second harmonic current distortion resulting from a dc-saturated convertor transformer.

There are several publications on the harmonic contribution of a saturated transformer. In 1978, Yacamini *et al.* showed that there is an approximately linear relationship between the resultant low order harmonics and the saturating dc current [Yacamini *et al.*, 1978]. They later applied this model to analyse the core saturation instability at the Kingsnorth scheme [Yacamini *et al.*, 1980b]. In 1986, Dommel *et al.* presented an iterative procedure to calculate low order odd harmonics resulting from symmetrical[2] transformer saturation [Dommel *et al.*,1986]. This technique was extended to include the effect of dc offset caused by the circulation of dc current in the transformer windings [Xu *et al.*, 1994]. However, this iterative approach has not been used to analyse the core saturation instability.

Another iterative technique has been developed [Watson *et al.*, 1994] that reveals the dependency of the resultant dc flux on the level of ac excitation already present in the core. It is shown that the resultant dc offset in the flux will push the core to almost the same level of saturation irrespective of the level of normal excitation.

In 1987, Stemmler developed an algebraic description of the saturation phenomenon and applied it in his analysis of the core saturation instability [Stemmler, 1987]. Based on his description, Wood extended the model to consider the sequence-dependent nature of the transformer saturation associated with the instability. He derived a worst case scenario of the transformer saturation for his study of the instability [Wood, 1993]. In 1994, Burton used electromagnetic transient simulations to determine the second harmonic contribution from the transformer saturation. The same simulation technique was used to predict the system susceptibility to the instability [Burton, 1994].

In this analysis, an algebraic transformer saturation model under the worst case scenario is first derived, based on the work of Wood and Stemmler. Time domain simulations similar to those used by Burton are then utilised to account for the effect of more realistic transformer magnetisation characteristics.

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[1] In practice, the harmonics are not exactly at the fundamental on the dc side, and exactly at the second harmonic and dc on the ac side, and this model can be adjusted to accommodate the slow variation described in section 3.3.

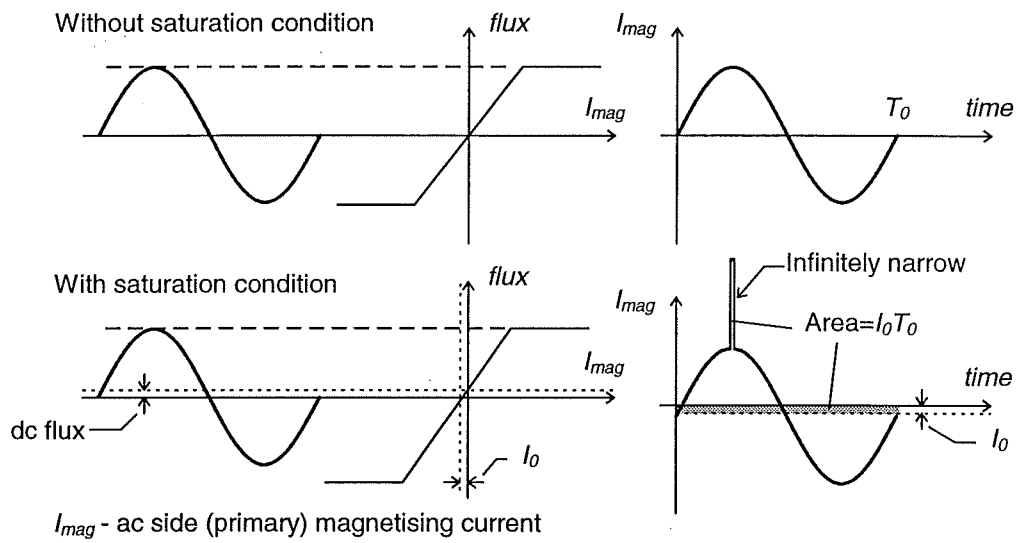
[2] Symmetrical implies no dc offset and the saturation effect is similar on both positive and negative half cycles.

3.5.1 Analytical model under worst case scenario

In the development of the convertor transformer core saturation instability, the saturating dc current impressed on the transformer is known to vary slowly as outlined in the previous sections. However, in this analysis, it is assumed that this variation is sufficiently slow to allow the assumption that the transformer is subjected to a true dc current. This assumption is needed here to derive a steady state transformer core saturation model.

To determine the convertor transformer core saturation harmonic contribution, firstly the effect of a dc current on the transformer magnetisation current is examined. It is best to consider the dc current on the transformer secondary, and the magnetisation current on the transformer primary. A single phase transformer is considered to start with.

Under the worst case conditions, the transformer magnetisation ac flux is assumed to be reaching the limits of the non-saturated part of its magnetisation characteristics as shown in Figure 3-5. Under such conditions, even a small dc bias will force an asymmetrical magnetisation current and cause transformer saturation to occur in one half of the fundamental cycle. Secondly, the worst case magnetisation characteristic of $I_{mag}/flux$ is assumed to be approaching infinite in the saturated region. This will cause the saturation current to have pulse shape as shown in Figure 3-5.



Note: The dc current (I_0) and the resultant dc flux are exaggerated in this figure.

Figure 3-5: Transformer operation under worst case condition

When there is no saturation, the transformer magnetising current flowing through its primary winding is sinusoidal as shown by the upper part of the figure. The flow of an infinitely low level of dc current I_0 on the transformer secondary will result in the presence of an infinitely low offsetting dc flux which causes distortion in the magnetising current (note that the levels of I_0 and corresponding dc flux are exaggerated in the Figure 3-5 for illustration purpose). This distorted current is made up of a sinusoidal part and an infinitely narrow impulse centred at the middle of one of the half cycles. As the sinusoidal part contains only the fundamental frequency, all of the distorting harmonics can be regarded as contained in the impulse. Therefore, the amount of positive sequence second harmonic current can be derived solely from the impulse part of the waveform.

In the steady state no dc will appear in the primary magnetisation current, so the area of the positive part of the magnetisation current must be equal to the negative part. Hence, the time integral of the saturation current pulse is equal and opposite to the time integral of the equivalent dc offset from the secondary side as shown by the dotted region in Figure 3-5. With the assumption of infinite $I_{mag}/flux$ in the saturated region, the duration of the saturation current pulse will be infinitely short allowing Fourier series of a periodic impulse train to be used to approximate the harmonic contribution from the dc saturation. In this analysis, only the second harmonic term of the Fourier series is taken into account, and other terms which may feed back through the convertor - dc system - convertor - ac system loop to become second harmonic are neglected.

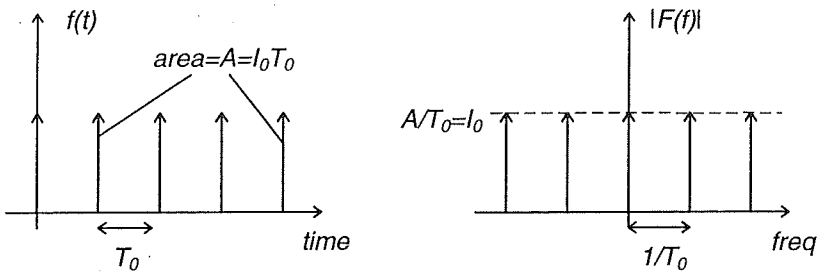


Figure 3-6: Frequency spectrum of the impulse train distortion

The Fourier Transform of an impulse train each with an area A and with a period of T_0 is a series of dirac delta functions separated by $1/T_0$ and weighted by A/T_0 as shown in Figure 3-6. With I_0 as the saturating dc current resulting in a time integral of I_0T_0, the second harmonic spectrum f_2 has the following amplitude response,

$$\left|F(f_2)\right| = \frac{A}{T_0} = \frac{I_0T_0}{T_0} = I_0 \tag{3.3}$$

This indicates a one-to-one relationship between the amplitude of the resultant second harmonic distortion and the saturating dc current.

The transformer magnetising current is in phase with the magnetising flux which is lagging the energising ac voltage by $T_0/4$ as shown in Figure 3-7. If the ac voltage is taken as the phase angle reference, the second harmonic component contained within the impulse of the distorted magnetising current will have the following phase angle response,

$$\arg\{F(f_2)\} = \pi \tag{3.4}$$

The frequency response depicted by equations 3.3 and 3.4 implies that under worst case scenario, a single phase transformer saturated by a dc current of amplitude I_0 will result in the generation of second harmonic current of similar amplitude but phase shifted by π radian. In order to find out the three phase relationship, both the saturating dc current and the resultant second harmonic current have to be extended to three phases.

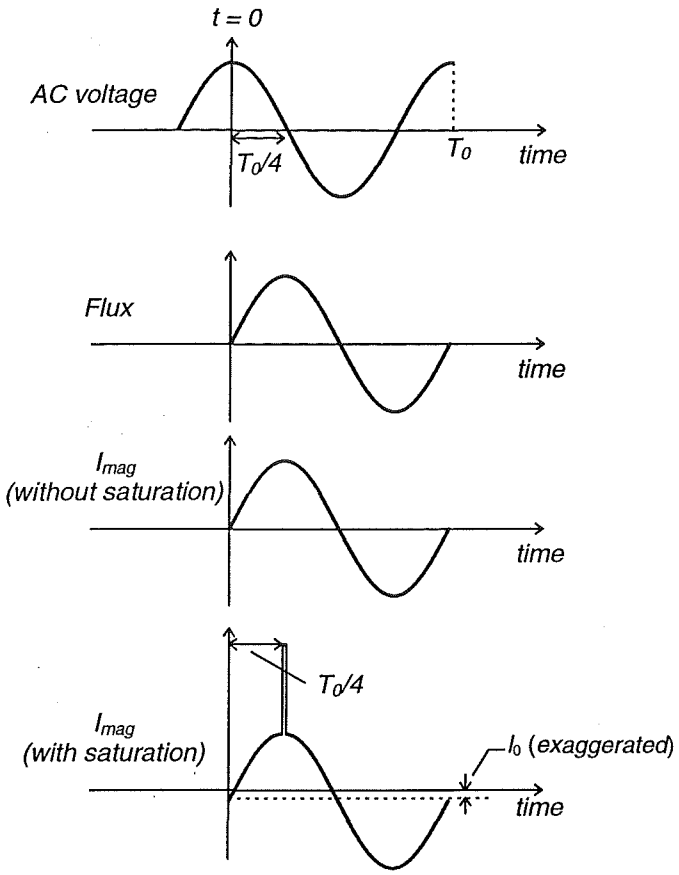


Figure 3-7: Phase difference between transformer magnetising current and ac voltage

The saturating dc current impressed on the transformer by the convertor as shown in Figure 3-2 can be expressed in the following negative sequence form,

$$I_{0-} = |I|\cos(\delta + \varphi) \quad , \quad \varphi = 0, \frac{2\pi}{3}, \frac{4\pi}{3} \tag{3.5}$$

where $|I|$ and δ are constant in time. From equations 3.3, 3.4 and 3.5, the second harmonic current absorbed by the convertor transformer for a dc current entering, or conversely the second harmonic current generated for a dc current leaving it (ie. the second harmonic current that results from transformer saturation), is

$$\begin{aligned} I_2 &= -2I_{0-}\cos(2\omega_0 t + \varphi) \\ I_2 &= -|I| \cdot \{\cos(2\omega_0 t + \delta - \varphi) + \cos(2\omega_0 t - \delta)\} \end{aligned} \tag{3.6}$$

The resultant second harmonic current consists of a positive sequence component and a zero sequence component. Only the positive sequence is involved with the development of the instability and thus needs to be taken into consideration,

$$I_{2+} = -|I| \cdot \cos(2\omega_0 t + \delta - \varphi) \tag{3.7}$$

Therefore if the frequency and phase sequence are taken as implicit in I_{2+} (positive sequence second harmonic current) and I_{0-} (negative sequence dc current) terms, then vectorially the relationship can be written as

$$I_{2+} = -I_{0-} \tag{3.8}$$

Therefore under the worst case conditions, the resultant positive sequence second harmonic current distortion on the transformer primary side has a similar amplitude to that of the saturating negative sequence dc current after it has been referred to the primary side, and is phase shifted by π radian.

3.5.2 *Effect of transformer magnetisation characteristics*

The one-to-one relationship of equation 3.8 was found to be too pessimistic and it is impossible to replicate this worst case scenario in dynamic simulations. Convertor transformers are usually over-designed and there is always a considerable margin before reaching the saturation region. Moreover, the I_{mag}/*flux* relationship in the saturation region is far from infinite as assumed in the worst case scenario. Therefore, the relationship between I_{2+} and I_{0-} will realistically be less than one, depending on the magnetisation characteristic of the transformer, ie.

$$I_{2+} = -X \cdot I_{0-} \quad , \quad 0 < X < 1 \tag{3.9}$$

Dynamic PSCAD/EMTDC simulations are utilised to approximate this ratio X. Using a three phase star-star transformer, energised at the primary side by a positive sequence ac voltage of nominal magnitude, a series of negative sequence dc currents are injected into the transformer

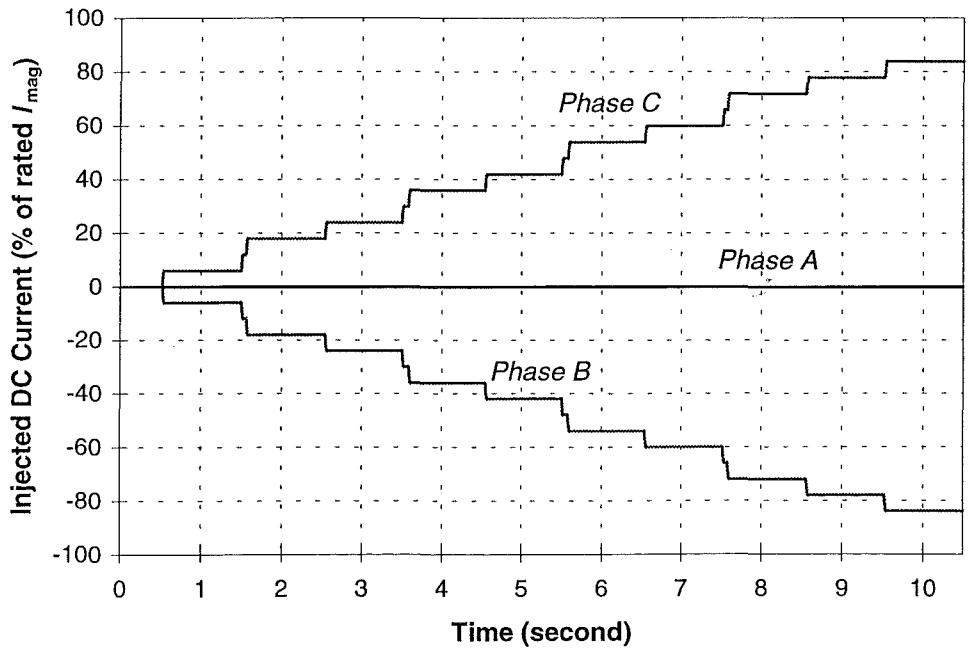


Figure 3-8: DC current injected into each phase of the transformer

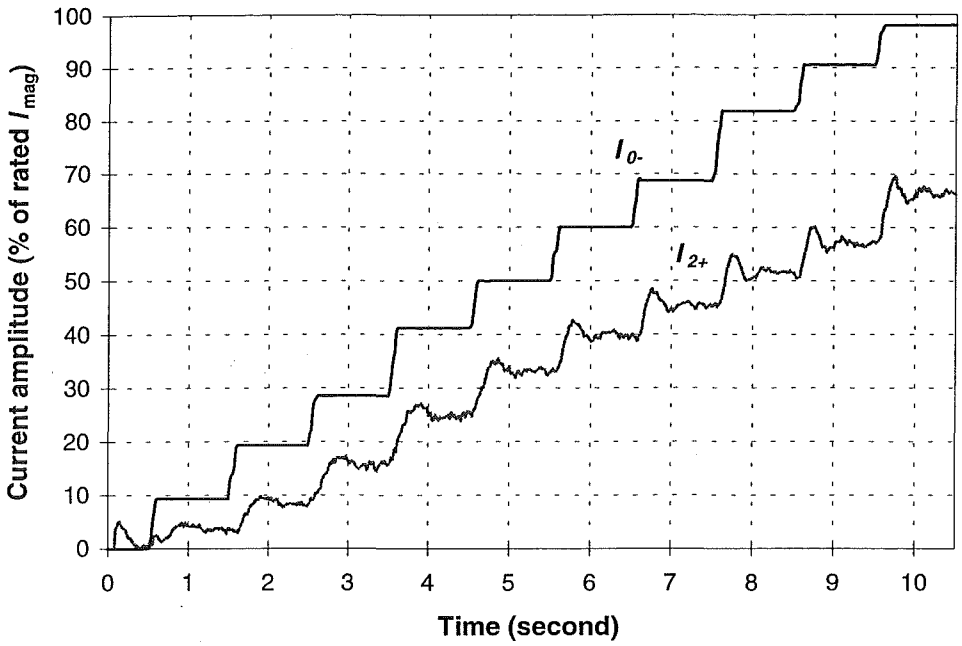


Figure 3-9: Amplitudes of the measured I_{2+} and the injected I_{0-}

secondary while measuring the amount of positive sequence second harmonic current flowing into the primary. The amplitude of the negative sequence dc current is ramped up in stages as shown in Figure 3-8 and Figure 3-9, and the corresponding amplitude of the positive sequence second harmonic current is plotted against it as shown in Figure 3-10. The dc injections are determined as percentages of the peak value of the transformer rated magnetising current, making the extent of the transformer saturation which is determined by the dc flux levels to correspond directly to the amount of injected dc currents. The measured values show a nearly linear relationship and by applying linear approximation, the slope of the curve is calculated as the ratio X for that particular transformer.

Figure 3-10 shows that at low negative sequence dc injections, corresponding to low transformer saturation levels, the measured values are less than the linear approximated values. The non-linear effect at low saturation levels is determined by calculating the value of X from the slope between the measured I_{2+} and the injected I_{0-} at each saturation level. The various values of X at different low saturation levels are summarised in Table 3-1 alongside the linear approximated values.

Table 3-1 also depicts the influence of the transformer knee point voltage level on the ratio X (with the transformer saturated reactance kept constant at 0.30 pu.). Transformers with higher knee point voltage will be less prone to saturation and hence result in lower harmonic contribution. The value of the ratio X will also vary according to other characteristics of the transformer including its levels of magnetising current and saturated reactance [Nayak *et al.*, 1994].

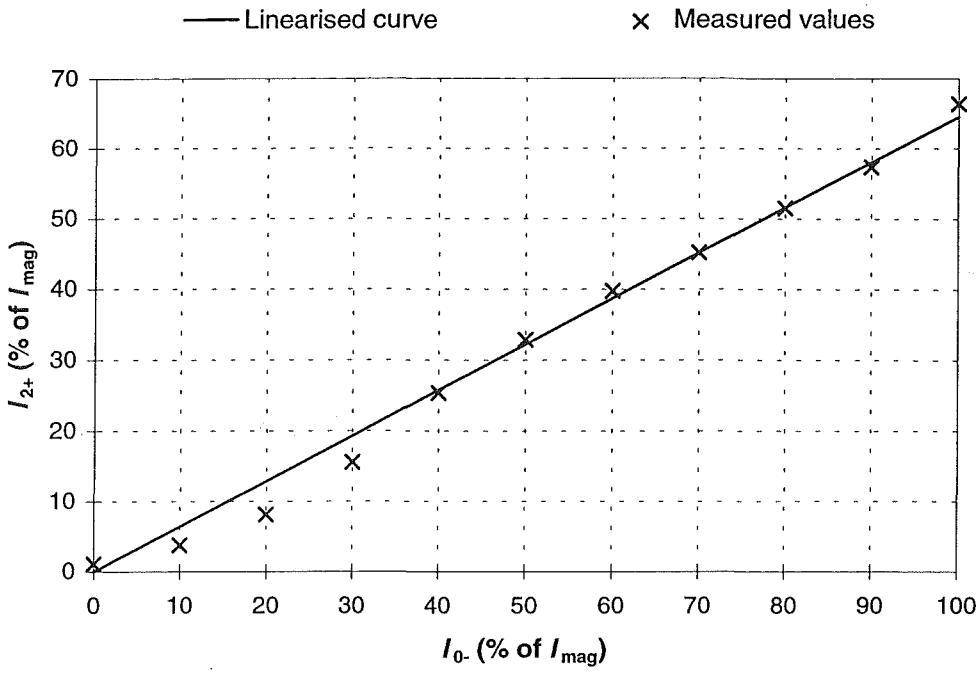


Figure 3-10: Measured and linearised I_{2+} versus injected I_{0-}.

Knee point voltage level (pu)	Injected I_{0-} (% of I_{mag})					Linear Approx.
	10	20	30	40	50	
1.05	0.51	0.60	0.80	0.92	0.96	0.85
1.15	0.38	0.47	0.63	0.74	0.80	0.74
1.25	0.33	0.42	0.53	0.60	0.65	0.65
1.35	0.32	0.38	0.49	0.51	0.55	0.56
1.45	0.29	0.37	0.43	0.46	0.47	0.49

Table 3-1: I_{2+}:I_{0-} ratios (X) at different saturation levels[3]

The above study has shown that the ratio X is strongly dependent not only on the transformer design but also on the level of saturation. Therefore, an approach is prescribed whereby the above procedure is applied to the particular transformer under analysis. The calculated transformer saturation gains of X are directly applied to the model to predict the system susceptibility to this instability.

3.6 Saturation Stability Factor

Based on the block diagram of the convertor transformer core saturation instability of Figure 3-3, the equivalent circuit used for the analysis of this type of instability is depicted in Figure 3-11. The convertor model is a 12-pulse convertor made up of two series connected 6-pulse

[3] Transformer saturation level defines the depth of the transformer saturation. It is equal to the dc-biasing current expressed as a percentage of the peak of the transformer rated magnetising current.

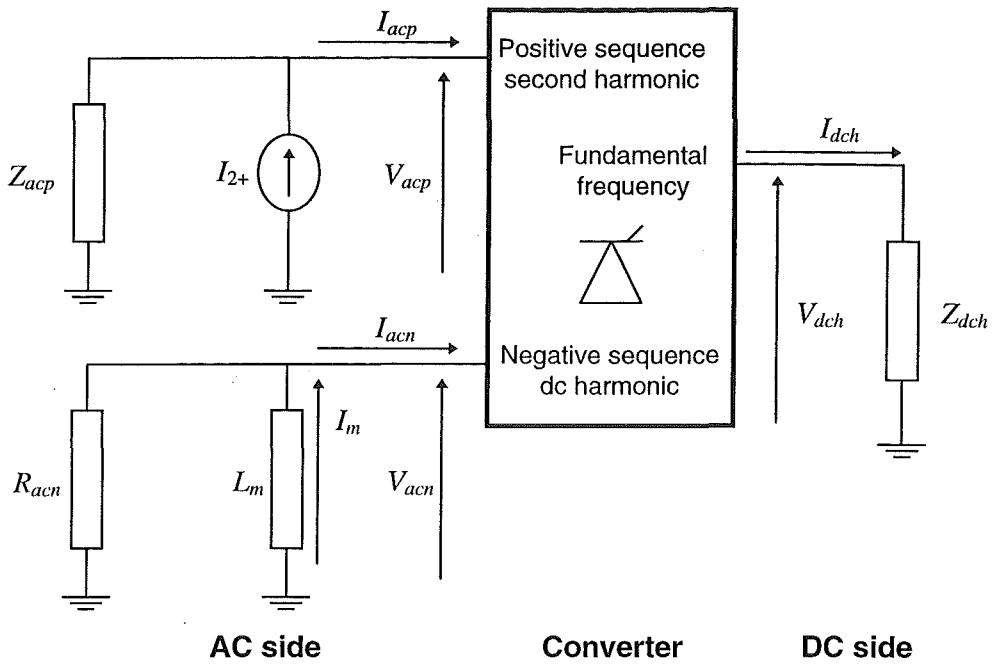


Figure 3-11: Equivalent circuit for the study of transformer core saturation instability

convertor bridges. The level of negative sequence current impressed by each of the bridges on the star/star and star/delta transformers is expected to be the same resulting in similar saturation effect from the transformers. The three frequencies considered in the equivalent circuit are the positive sequence second harmonic and the negative sequence dc on the ac side, and the fundamental frequency on the dc side. Although the harmonic voltage and current distortions are sequence-dependent, the two ac networks are simply the impedance of the ac system at the respective frequencies.

In positive sequence, the second harmonic current flowing through the ac side second harmonic impedance of Z_{acp} is made up of the difference between the I_{acp} impressed by the convertor and I_{2+} from the transformer saturation. The I_{2+} is calculated using equation 3.9 according to the level of negative sequence dc current that is saturating the convertor transformer. This saturation current is represented by the amount of the negative sequence dc current I_{acn} from the convertor that is flowing into the transformer magnetising inductance L_m. L_m is actually non-linear but the transformer is only in saturation for a short period of each fundamental cycle, as indicated by the width of the impulse part of the distorted magnetising current in Figure 3-5. Therefore, it is reasonable to assume L_m as the unsaturated magnetising reactance, as indeed it has this value most of the time. The non-linear effect of the saturation is included as a positive sequence second harmonic current injection of I_{2+} as outlined above.

In previous models including that of [Wood, 1993], I_{acn} was taken as true dc and thus, none of it would pass through the convertor transformer and none would appear in the ac system. All of I_{acn} was assumed to flows into L_m, saturating the transformer core and contributing to I_{2+}. However, this assumption was found to be too pessimistic overestimating the likelihood of such an instability. Therefore, in this analysis, I_{acn} is considered to be varying as part of the growth or decay of the process, and hence part of it will pass through the transformer and flow into the ac system. As a result, the path for this I_{acn} consists of the transformer magnetising inductance in parallel to the ac system impedance at the low frequency of the I_{acn} variation. Assuming that the ac system impedance remains fairly constant around 0Hz, this

effect can be represented by connecting the ac system resistance at 0Hz (R_{acn}) in parallel with the transformer magnetising inductance as in Figure 3-11. On the dc side of the convertor, the equivalent impedance Z_{dch} is made up of the fundamental frequency impedance of the dc system and the equivalent impedance of the remote end convertor with the connected ac networks.

In addition to the linearised convertor transfer function of equation 3.2, describing the convertor operation, a set of simultaneous complex equations is written to describe this equivalent circuit,

$$\begin{aligned} V_{acp} &= -I_{acp} Z_{acp} + I_{2+} Z_{acp} \\ I_{2+} &= -X.I_m \\ I_m &= I_{acn} + \frac{V_{acn}}{R_{acn}} \\ V_{acn} &= -L_m \frac{dI_m}{dt} \\ V_{dch} &= I_{dch} Z_{dch} \end{aligned} \tag{3.10}$$

Expressing the negative sequence dc current I_{acn} in the exponential vector form $I_{acn}^{t=0}.e^{-(\alpha+j\beta)t}$ with $I_{acn}^{t=0}$ as the initial condition and including the magnitude and phase responses, the response of the core saturation stability feedback loop is indicated by the α and β terms. The above equations are solved simultaneously and the exponential terms of α and β are obtained as functions of the harmonic impedances and the frequency coupling terms of the matrix in equation 3.2.

$$\begin{aligned} I_{acn} &= I_{acn}^{t=0}.e^{-(\alpha+j\beta)t} \\ \alpha + j\beta &= \frac{R_{acn}}{L_m}.\frac{\left(1 + A.Z_{acp} + X.C.Z_{acp}\right)}{\left(\left(1 + R_{acn}.D\right).\left(1 + A.Z_{acp}\right) - R_{acn}.B.C.Z_{acp}\right)} \\ A &= d + \frac{f.a}{Z_{dch} - c} \\ B &= e + \frac{f.b}{Z_{dch} - c} \\ C &= g + \frac{i.a}{Z_{dch} - c} \\ D &= h + \frac{i.b}{Z_{dch} - c} \end{aligned} \tag{3.11}$$

The term α is defined as the *Saturation Stability Factor* (*SSF*) [Wood, 1993] which basically defines the susceptibility of the system to the development of this type of instability[4]. A positive *SSF* value indicates that the harmonic sequence will decay over time and hence the

[4] A system is stable if the roots of its characteristic equation have a negative real part (ie. $e^{(\alpha+j\beta)t}$ with a negative α term) [Nagrath *et al.*, 1986] page 185.

system is stable. On the other hand, a negative *SSF* suggests negative damping and the development of instability as the distorting harmonic sequence increases over time. The value and sign of the β term determine the speed and the direction of the variation of these harmonic sequences. The properties of both of these terms are revealed and explained using dynamic time domain simulations in the following sections. Although I_{acn} is used in this derivation, the other relating harmonic sequences of V_{acn}, V_{acp}, I_{acp}, V_{dch} and I_{dch} can be equally used and a similar result will be achieved.

The *SSF* formulation has included the transformer saturation contribution to the gain of the instability feedback loop. This contribution is regarded as the transformer saturation gain and is quantified as the I_{2+}:I_{0-} ratio X in equations 3.9 and 3.11. In section 3.5.2, it was shown that due to the non linear magnetisation characteristics of the convertor transformer, this contribution will increase with the saturation levels. Therefore, the value of this contribution to be applied to the *SSF* calculation depends on the type of core saturation instability under consideration.

The two types of core saturation instability introduced in section 3.1, ie. spontaneous and kick-started, differ from each other in the starting point, defined by the level of transformer saturation. In this analysis, the transformer saturation gain of X is calculated according to the saturation level expected at the starting point. For the spontaneous instability, the considered saturation level is low, around 10-20% depending on the amount of residual saturation expected in the system. At these low saturation levels, the ratio X is calculated directly from the slope between the measured I_{2+} and the injected I_{0-}. On the other hand for the kick-started version a the linear approximated ratio of X, as derived in section 3.5.2, is used. Both of these types of core saturation instability are illustrated using the *SSF* technique and validated with dynamic simulations in the following sections.

3.7 Validation of SSF with dynamic simulations

For the purpose of validating the proposed *Saturation Stability Factor* (*SSF*) as a means to measure the system susceptibility to core saturation instability, two simplified HVDC systems are set-up on the transient simulation program, PSCAD/EMTDC. Both systems are adapted from the test system used by Burton [Burton, 1994] which is described in Appendix B. They both consist of a 12-pulse rectifier with RLC equivalent circuits representing the ac and dc systems as shown in Figure 3-12. A constant current controller implemented as proportional and integral controller is used on the rectifier while the invertor is simplified to a voltage source. The details of the ac and dc systems, the proportional gain and integral time constant of the convertor controller are summarised in Table 3-2. The *SSF* values of the systems are

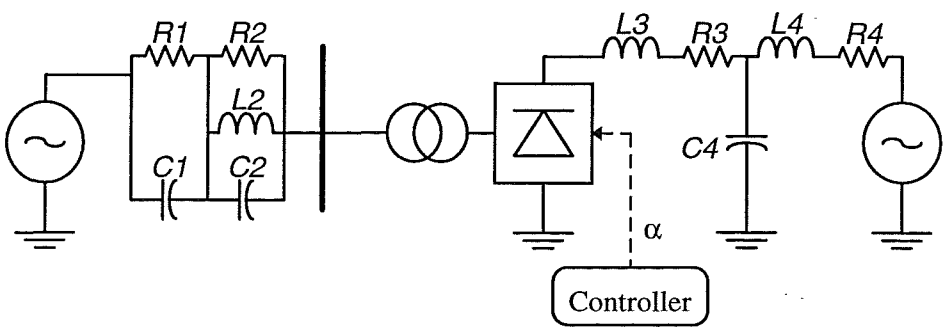


Figure 3-12: Schematic of the test systems

calculated first and the predictions are validated against the time domain EMTDC simulations.

	System 1	*System 2*
Resistance at ac side at 0Hz, R_{acn} (ohms)	100.0	100.0
Second harmonic admittance on ac side, $1/Z_{acp}$ (mhos)	0.001 -j0.004	0.002 -j0.001
Fundamental frequency admittance on dc side, $1/Z_{dch}$ (mhos)	0.0 +j0.010	0.0 +j0.010
R1 (ohms)	100.0	100.0
C1 (μF)	1200.0	1200.0
R2 (ohms)	1030.0	501.32
L2 (mH)	6.291	6.3471
C2 (μF)	396.31	397.49
R3 (ohms)	0.0	0.0
L3 (mH)	600.0	600.0
R4 (ohms)	1.0	1.0
L4 (mH)	918.0	918.0
C4 (μF)	22.0668	22.0668
Proportional Gain (Radian/kA)	0.4540	0.4540
Integral time constant (second)	0.0036	0.0036

Table 3-2: Details of the test systems used for validation of *SSF*

The first system is fabricated to have negative *SSF* values to demonstrate the development of both types of core saturation instability. In the second system, the ac side equivalent circuit is altered so that the system becomes stable with a positive *SSF* value.

3.7.1 Spontaneous core saturation instability

Saturation level	*X* ratio	*SSF*
20%	0.60	-0.23
30%	0.80	-2.05
40%	0.92	-3.15

Table 3-3: *X* ratios and *SSF* values of the test system 1 at different saturation levels

The knee point voltages of the convertor transformers in the first system are lowered to 1.05 pu to demonstrate the development of spontaneous type of core saturation instability. At low saturation level of about 20%, Table 3-1 shows that the I_{2+}:I_{0-} ratio is about 0.6 resulting in a negative *SSF* value of -0.23 for the system. This indicates that with the presence of about 20%

of residual saturation in the convertor transformer, the instability feedback loop gain is negative and the small saturation will develop into an instability. Furthermore, the increased ratio with transformer saturation level causes further lowering of the *SSF* values as summarised in Table 3-3.

The EMTDC simulation results in Figure 3-13 confirm the presence of the spontaneous type of core saturation instability. After the initial ramp-up and allowing the system to settle for about 0.5 second, the amount of negative sequence dc component within the transformer magnetising current is found to be about 20% of the rated magnetising current. A low negative *SSF* value suggests a slow growth in the saturation level and in the harmonic distortions as depicted in the results. As the instability develops, the saturation increases raising the transformer saturation gain and further lowering the system *SSF* value. This results in the acceleration of the development of the instability as indicated by the larger increase in the amplitude of the saturating dc current between the time of 3 and 4 second.

The EMTDC simulation described above clearly depicts the classical case of core saturation instability. It not only confirms the "grow-from-nothing" nature of this type of harmonic instability, but also shows that as the saturation develops the effect of the transformer will increase concurrently accelerating the development of the instability.

The waveforms of the transformer magnetising current show that the three phases are not dc-biased to the same offset level, and the saturating dc current has a negative sequence manner. The figures also show the increase in amplitude and the rotation of the saturating negative sequence dc current with the development of the instability. The direction and speed of these rotations are further clarified in section 3.7.3.

3.7.2 Kick-started core saturation instability

The transformer knee point voltage was returned back to 1.25 pu. reducing the saturation gain to 0.42 at 20% of saturation. This eliminates the spontaneous type of instability from the system. However, if the transformer is heavily saturated (>100%), the linear approximation effects a gain of 0.65 making the *SSF* negative at -0.68. This suggests that if the system is subject to certain external stimulus causing the transformer to become heavily saturated, the core saturation instability will eventuate. The test case is simulated to 1 second when a ±2.5° of modulation at the fundamental frequency was introduced to the convertor firing angle order. This causes the convertor to impress a negative sequence dc current on the transformer secondary. The modulation was removed at 1.5 second when the saturating dc current has reached about 200% of the rated magnetising current. Full detail of this modulation process is described in Appendix B. With the extraneous modulation removed, the system stability is determined from its ability to settle back to its original pre-disturbance conditions.

The simulation results in Figure 3-14 confirms the presence of kick-started type of core saturation instability in the second system. After 1.5 second, the saturating dc current continues to rise even though the inducing modulation has been removed. This implies that the induced saturation has reached sufficient level to kick-start the instability. Furthermore, the magnetising currents show a pseudo-sinusoidal variation alongside the increase in the saturating dc current. This observation further validates the vector form of solution proposed in this *SSF* approach (equation 3.11) that the distorting harmonic sequences not only vary in their magnitudes but will also rotate over time. In this system, the vector rotation β term is -0.30 suggesting that the negative sequence I_{acn} vector rotates in the anti-clockwise direction.

This prediction corresponds to the simulation results where the order of rotation is phase A followed by phase C and then B.

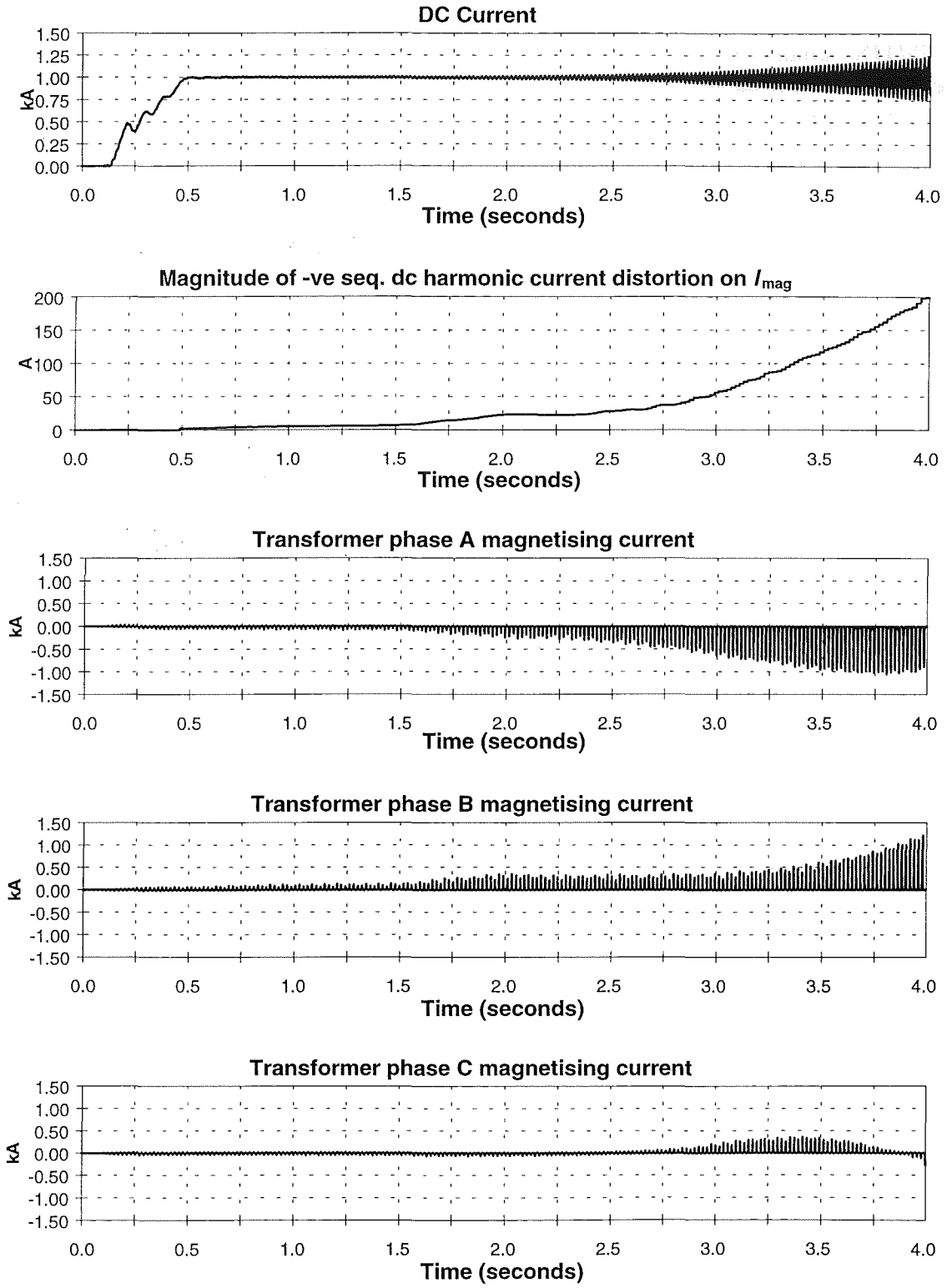


Figure 3-13: Simulation results of spontaneous core saturation instability

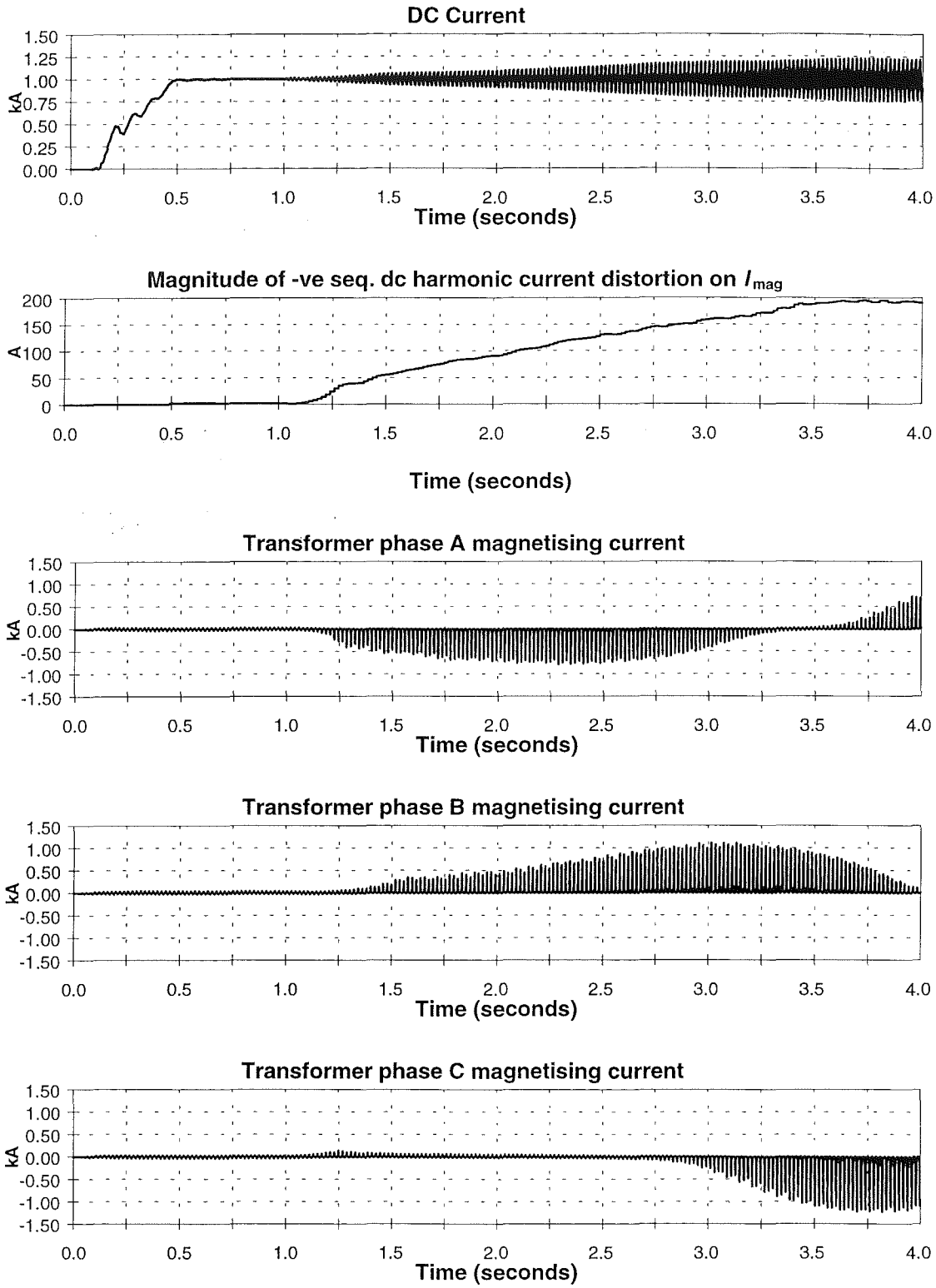


Figure 3-14: Simulation results of kick-started core saturation instability

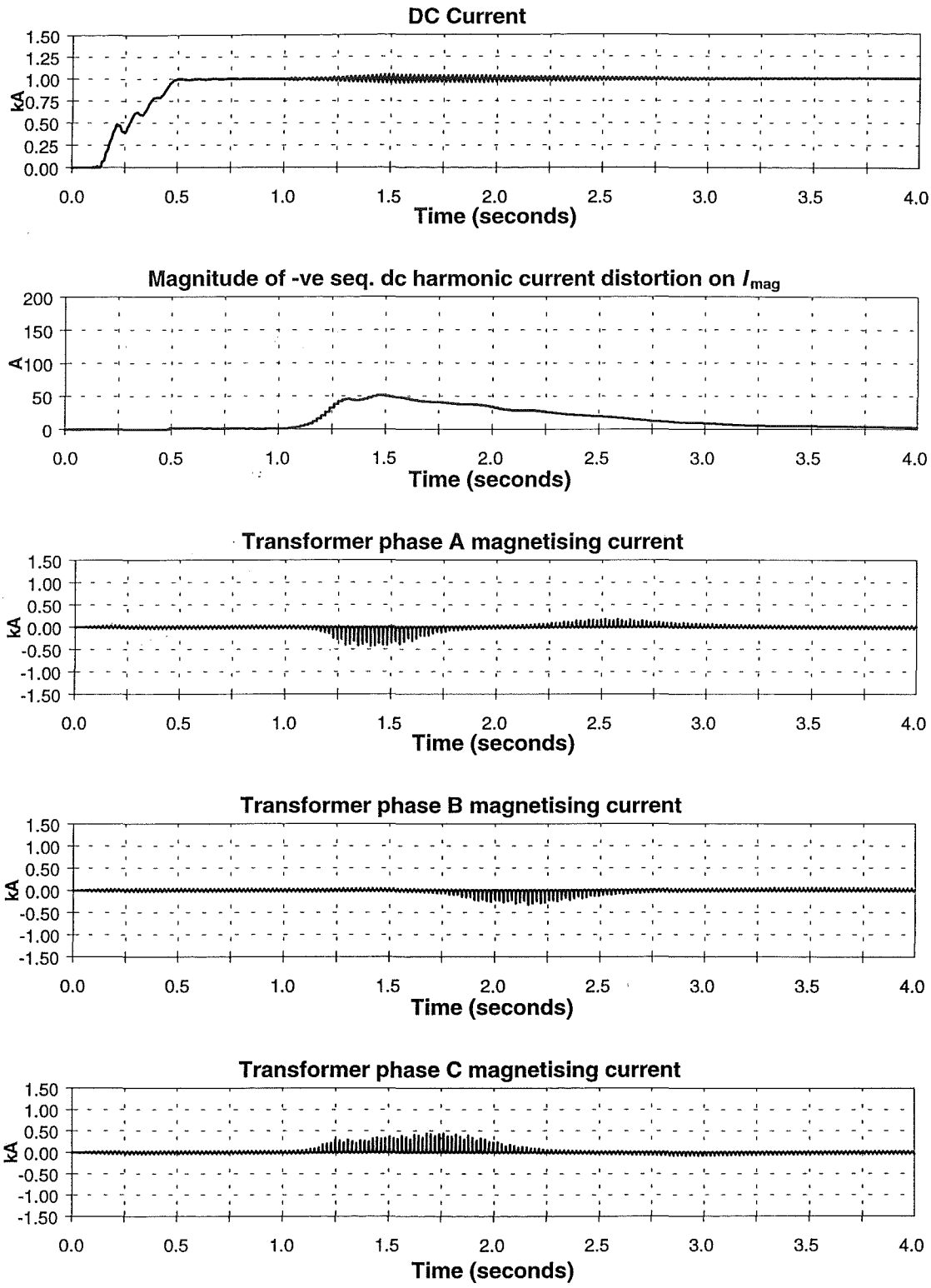


Figure 3-15: Simulation results of stable system with positive *SSF*

3.7.3 Stable system with positive SSF

In the second system, the ac side impedance is altered so that the system *SSF* value becomes positive. Similar transformers were used with the *X* ratio of 0.65 and the resultant system *SSF*

is 2.19. This implies that the system should not develop core saturation instability even if the transformer is kick-started with high saturation levels. On the contrary, the high *SSF* value should see the harmonic distortions die away quickly.

The corresponding simulation results of this second system are shown in Figure 3-15. In the simulation, the convertor is subjected to similar firing angle modulation as in the previous case resulting in about 200% of transformer saturation before it is removed. However, instead of developing into an instability, the harmonic distortion on both ac and dc sides decreases with the decline in the transformer saturation. This observation confirms the prediction from the positive *SSF* value that the system is stable.

Although the susceptibility of a system to the instability depends solely on the α in equation 3.11 or the *SSF* term, it is interesting to demonstrate the additional information provided by the β vector rotation term. The close agreement with EMTDC simulations in predicting the rotation acts as further confirmation to the direct frequency domain model and the simplified transformer saturation model used in the analysis. In this stable system, β is +2.56, implying that the vectors rotate in a clockwise direction. The negative sequence form of I_{acn}, coupled with the slow negative rotation of the vector, leads to the dc component of the transformer magnetising current varying in the phase order A, B, C. This is confirmed by the EMTDC simulation.

3.8 Discussion

The illustrations above only show the effect of the sign of the *SSF* α term and vector rotation β term which respectively determine if the system is stable or otherwise and the direction of the vector rotation. However, the absolute values of these terms actually dictate the rate of change in the amplitudes of the distorting harmonics and the speed of their vector rotation. In Table 3-4, the values of these terms calculated using the direct frequency domain method (*SSF*) are compared to those extracted from the EMTDC simulations.

System	Direct frequency		EMTDC simulation	
	α (sec^{-1})	β (rad/sec)	α (sec^{-1})	β (rad/sec)
1	-0.68	-0.30	-0.66	-0.59
2	2.18	2.56	1.24	2.21

Table 3-4: Comparison of α and β terms from *SSF* and EMTDC simulations

The differing values in the table indicate some discrepancies between the two approaches. It must be remembered that a number of approximations have been made in order to preserve the simple direct solution in the analysis. The linearised convertor transfer function of equation 3.2 has been found to have good agreement with EMTDC simulation in the magnitude response but there are some differences in the phase response [Wood, 1993]. The development of this type of instability requires the feedback harmonic sequences to be in-phase with the original component, and thus any discrepancy in the prediction of the phase response will be propagated into the *SSF* and vector rotation values.

Despite these differences, the two methods agree on the relative stability of the system. A higher *SSF* value will most certainly be accompanied by a greater damping in the EMTDC simulation.

3.9 Conclusion

This chapter has examined in some detail the mechanism of convertor transformer core saturation instability. A term, called *Saturation Stability Factor* has been proposed to give a measure of the system susceptibility to this type of instability. Validation with time domain simulation has provided sufficient agreement to give confidence in the linearised frequency domain model. The technique has been shown to be accurate in predicting both the spontaneous and kick-started types of core saturation instability.

Being a direct frequency domain approach, this technique has the advantage of quick solutions and low computational burden. It should prove a useful tool in providing a general overview of the entire instability problem. With this approach, the properties commonly possessed by systems with this type of instability can be determined and this should raise the level of understanding of the factors contributing to it. Furthermore, the relative stability of different systems is easily derived allowing the design of system components including the convertor controller to be optimised to prevent the development of core saturation instability.

Chapter 4

Characteristics of Core Saturation Instability

4.1 Introduction

The direct frequency domain *SSF* approach described in the previous chapter possesses great potential for the evaluation of the properties exhibited by systems prone to convertor transformer core saturation instability. Its minimal computational burden and hence quick solution provides an effective way of investigating the system characteristics under such unstable conditions. With the use of linear approximation and a direct solution, each individual factor can be easily altered to unravel its particular effect on the instability mechanism. Furthermore, by considering several factors simultaneously, it is possible to find out the dominant factor contributing to the build up of the instability.

Among the various characteristics considered in this study are the harmonic impedances of the connected ac and dc networks. The *SSF* formulation includes the resistance at 0 Hz and the second harmonic impedance of the ac system, and the dc system impedance at the fundamental frequency. Sensitivity studies were undertaken on each of these impedances to find out their effects on the system stability. Their individual effects were then combined to reveal the dominant character.

Besides the system impedances, the effect of using convertor transformer with different magnetisation characteristics is also investigated. It is expected that the likelihood of this instability is closely coupled to the transformer susceptibility to core saturation.

The action of the convertor controller affects the amount of frequency transfer between the ac and dc side of the convertor. This in turn affects the development of the instability. The frequency response of the convertor controller at the relevant frequencies is evaluated and applied to the *SSF* formulation. Although a wide range of controller characteristics are analysed, most of the effort is concentrated on the response of the widely used constant current controller. Besides looking at the influence from the controller itself, its impact on the effects of other parameters to the instability is also analysed. One of the major aims of this study is to assess if there exists a general solution to this type of instability, perhaps through proper tuning of the convertor controller frequency response.

Lastly, the effect of operating the convertor at different firing angles and different commutation angles is studied. Changes to the firing angle not only affect the system stability by its own accord, but also the commutation process, which in turn causes further effect on the system stability.

The analysis is carried out initially with the convertor operating in rectification mode. The same method is then applied to the invertor and the results are presented in the latter part of

the chapter. Finally, all the findings are brought together to assess the implications on both the conventional HVDC scheme with long dc transmission line and the back-to-back intertie.

4.2 System impedances

This section assesses the impedance profiles of the ac and dc systems in an unstable HVDC scheme. The considered impedances are the three components used in the formulation of *SSF* namely the ac side resistance at 0 Hz, dc side impedance at the fundamental frequency and the ac side second harmonic impedance. There are two major issues being investigated in this section. Firstly, the characteristics of these impedances that lead to unstable systems are evaluated. The second point concerns the effect of the variations in these harmonic impedances on the *SSF* and hence on the system stability. This latter analysis determines how each impedance affects the system stability and provides useful guidelines for determining preventive or control solutions. The effect of individual impedances is considered first and this is followed by a summary of their combined effects. A full description of the analysis of their combined effects is presented in Appendix C.

4.2.1 AC side resistance at 0 Hz

The same simplified test system used in the previous chapter and explained in Appendix B (Figure B-1) is used in this investigation. Ignoring the action of the convertor controller and representing the invertor as a constant current source, the rectifier firing angle is locked at 20 degrees. The ac side second harmonic admittance and the dc side fundamental frequency impedance are held constant while the ac side resistance is varied from 50 ohms to 500 ohms and the corresponding *SSF* is calculated.

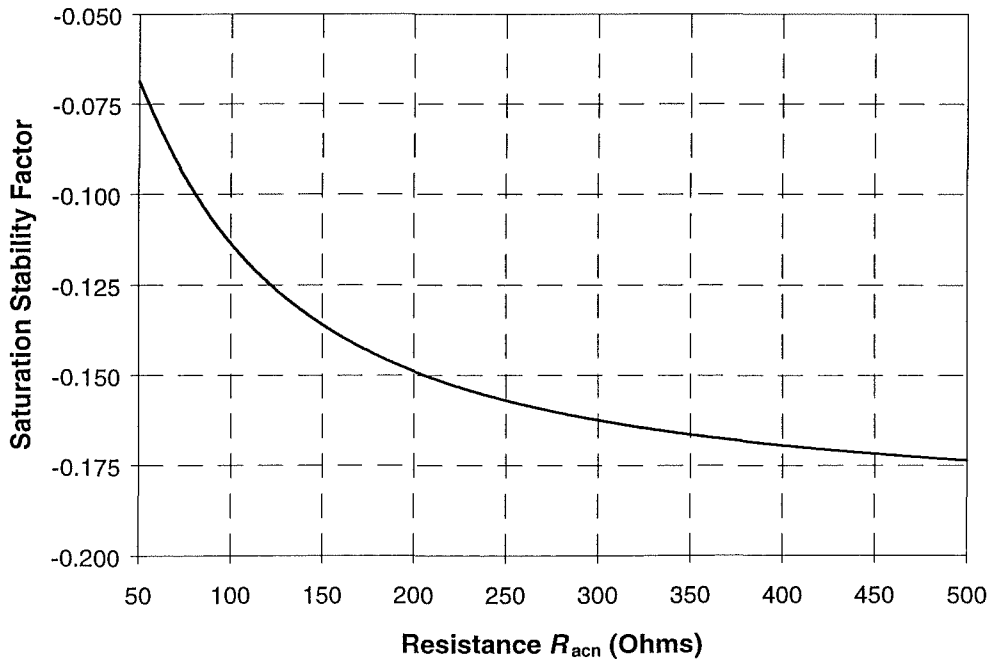


Figure 4-1: *SSF* versus ac side resistance

Figure 4-1 shows that the *SSF* reduces as the ac side resistance increases. This resistance forms a parallel branch with the transformer magnetising inductance for the flow of the negative sequence dc current generated at the convertor. A high resistance sees most of the dc current to flow into the magnetising inductance and thereby saturate the transformer. This enhances the development of the instability as indicated by the lowering of the *SSF*. This observation shows that the traditional view of higher resistance resulting in greater damping and subsequently more stable system is not always true. On the contrary, core saturation instability is more likely to occur on systems with high ac side resistance.

However, the variation in *SSF* is very small (less than 0.1) over the range of resistance considered. This suggests that the effect of ac side resistance may be of less significance and its effect may be nullified by other parameters such as the second harmonic impedance. Furthermore, the *SSF* approaches constant value as the resistance increases implying that its effect on the system stability has decreased. This is because the sufficiently high resistance has already caused most of the dc current to saturate the transformer, and therefore any further increase in the resistance will not raise the saturation level and the system susceptibility significantly.

4.2.2 AC side second harmonic impedance

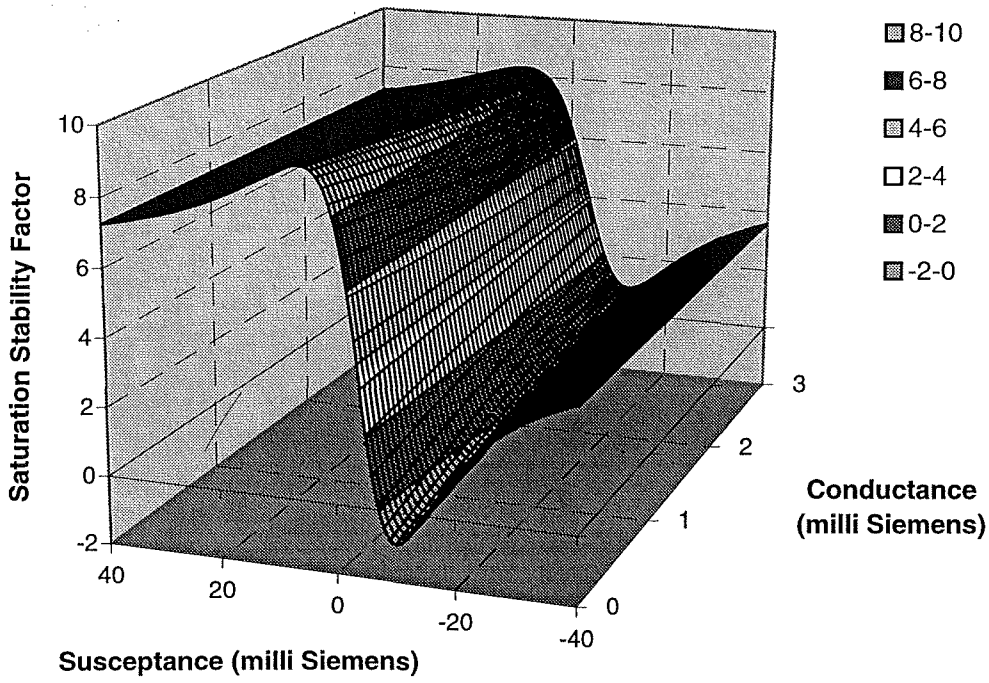


Figure 4-2: *SSF* versus ac side second harmonic admittance

In the development of the convertor transformer core saturation instability, there are two major sources of positive sequence second harmonic current flowing into the ac system. The first source originates from the convertor dc side and involves the switching action of the convertor. Any fundamental frequency current distortion flowing on the convertor dc side will be transformed to a positive sequence second harmonic component on the ac side. Furthermore this distortion may be picked up by the convertor controller which, through its firing angle modulation, produces additional positive sequence second harmonic current on

the ac side. Secondly, the saturation on the convertor transformer causes among other characteristic and non-characteristic harmonic currents, the positive sequence second harmonic current to flow on its primary or line side. All of these currents "add-up" and flow through the ac system impedance resulting in a corresponding positive sequence second harmonic voltage distortion. The convertor in turn transforms the voltage distortion to further fundamental frequency distortion on the dc side, completing the instability feedback loop. Therefore, it is expected that a high second harmonic impedance at the ac side will result in high harmonic voltage distortions being fed back to the dc side and hence the more likelihood of developing such an instability.

This analysis is carried out by calculating the system *SSF* for different values of the ac side second harmonic impedance while keeping other parameters unchanged. For the ease of analysis and presentation, the second harmonic admittance (conductance and susceptance) is used instead of the impedance (resistance and reactance). The admittance is varied from 0.0-j40 to 3.0+j4.0 milli Siemens and the resulting *SSF* is plotted as a three dimensional surface in Figure 4-2. The variation in the *SSF* value depicts the influence the ac side second harmonic impedance has on the system core saturation stability. The *SSF* was observed to vary significantly only within the range of admittance considered above, and beyond this region it tends to constant values according to the contours shown in the figure.

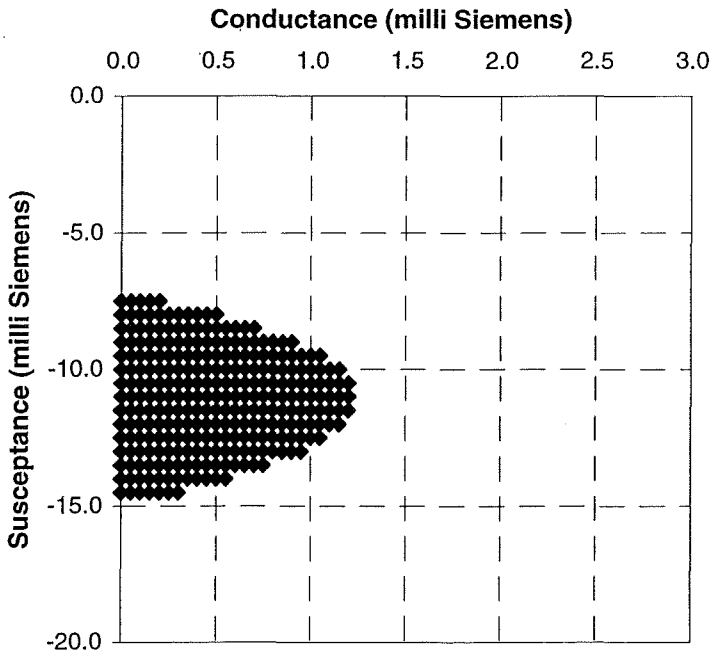


Figure 4-3: Range of ac side second harmonic admittance with negative *SSF*

The unstable condition is indicated by the range of admittance where the *SSF* is negative. This range of admittance is shown with a scatter plot in Figure 4-3. The system stability was expected to be poorest when the impedance is high, which corresponds to near zero admittance. However, the analysis indicates that this is not so, as the region with negative *SSF* is slightly away from the zero susceptance axis. The instability region congregates around a negative susceptance of about -10 milli Siemens, where the ac system including the harmonic filters and the compensation capacitors is inductive at the second harmonic. This suggests the presence of a parallel resonance on the ac side near the second harmonic but at a

frequency slightly higher than the second harmonic frequency. It is also noted that for this specific case, there is no instability region in the positive susceptance half where the ac system is capacitive at this frequency.

In Figure 4-3, the unstable region narrows with the increase in the conductance, suggesting that the conductance always contributes positively to the damping of the instability feedback loop. On the other hand, the increase (from negative to positive) of the susceptance sees both increases as well as decreases in the *SSF*. Figure 4-4 shows the variation of *SSF* as the susceptance is varied from -40 to 40 milli Siemens. Beyond this range of susceptance, the *SSF* approaches constant positive values indicating stability. The *SSF* is only negative around the susceptance of -10 milli Siemens. This suggests the aforementioned remark that the core saturation instability will only develop in systems having an inductive ac side at the second harmonic frequency. Besides that, the curve also shows the sensitivity of the system stability to changes in the susceptance. The closeness of the dots on the curve indicates that it is relatively insensitive to changes in the ac side second harmonic susceptance except between -10 and 0 milli Siemens. Between these two susceptances, a small change in the ac side second harmonic susceptance, such as removing a harmonic filter from operation, may drop the system *SSF* to below zero rendering the system to be prone to the core saturation instability. Therefore, it would be advisable to operate the system away from this area of susceptance so as to minimise the chances of falling into the unstable condition. This observation reinforces the capability of the *SSF* approach in revealing problematic regions and thereby assists in avoiding the core saturation instability.

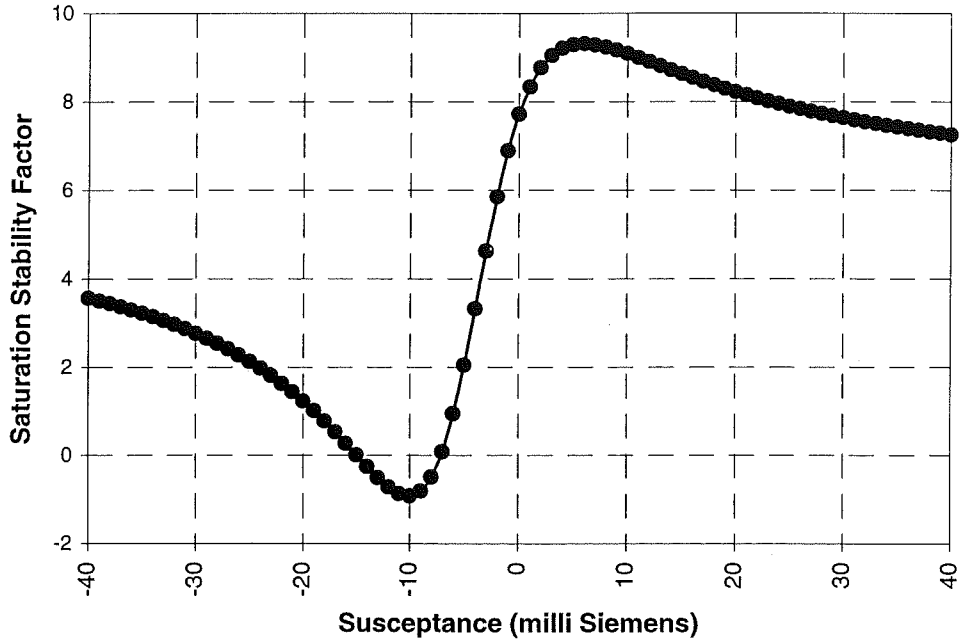


Figure 4-4: *SSF* versus ac side second harmonic susceptance

4.2.3 DC side fundamental frequency impedance

The last harmonic impedance to be considered is the dc side impedance at the fundamental frequency. The switching action of the convertor which transforms the fundamental frequency

voltage on the ac side to the intended dc voltage on the dc side inadvertently also transforms any positive sequence second harmonic voltage distortion on the ac side to a corresponding fundamental frequency voltage distortion on the dc side. Therefore, the presence of positive sequence second harmonic voltage distortion on the ac side as a result of the transformer saturation will cause a fundamental frequency voltage distortion on the dc side. As a result, the dc current will be distorted by a fundamental frequency component. The level of this current distortion depends on the size of the dc side impedance. Via the same convertor switching action, this current distortion will be transformed back to the ac side as a positive sequence second harmonic current and a negative sequence dc current. If the dc side impedance at the fundamental frequency is low, the resulting current distortion will be high and so will the corresponding distortion being fed back to the ac side. Hence, it is anticipated that HVDC systems with low dc side fundamental frequency impedance will be more susceptible to the core saturation instability.

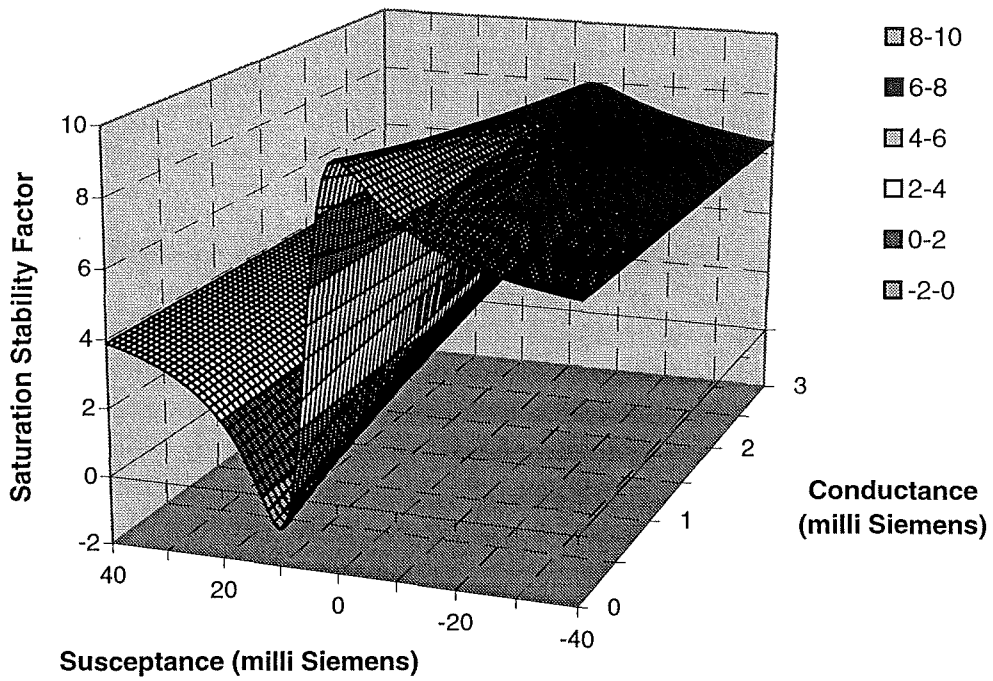


Figure 4-5: *SSF* versus dc side fundamental frequency admittance

The same technique used to study the effect of the ac side second harmonic impedance is used here to investigate the effect of the dc side impedance. The *SSF* of the test system is calculated for several dc side admittances ranging from 0.0-j40 to 3.0+j40 milli Siemens while keeping other parameters constant. Figure 4-5 depicts the three dimensional plot of the calculated *SSF* versus the dc side admittance. This particular surface resembles the mirror image of that plotted against the ac side second harmonic admittance in Figure 4-2. The unstable region with negative *SSF* falls on the positive half of the susceptance as shown in Figure 4-6. This suggests that a system experiencing core saturation instability has a dc side which is capacitive at the fundamental frequency. Furthermore, there is no unstable region in the negative half of the dc side fundamental frequency susceptance. These observations imply that in a system prone to core saturation instability, there is a series resonance on the dc side near the fundamental frequency but at a frequency slightly higher than the fundamental frequency.

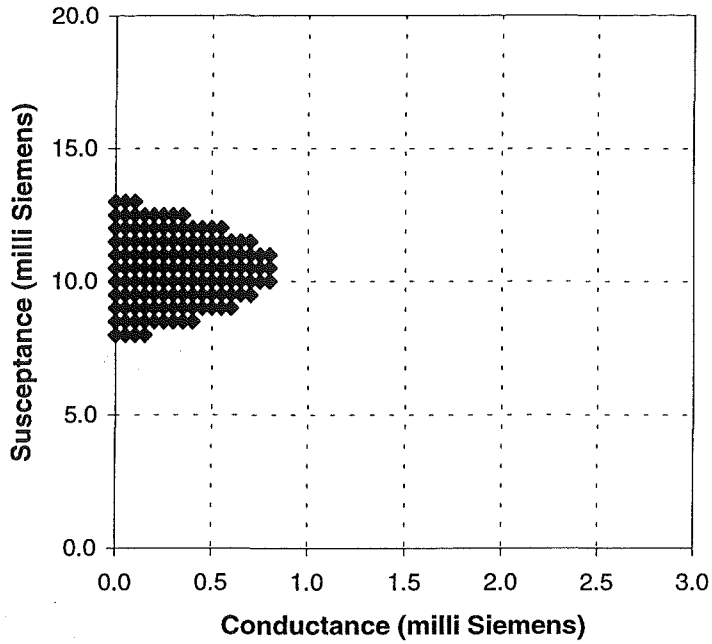


Figure 4-6: Range of dc side fundamental frequency admittance with negative *SSF*

Figure 4-6 shows that the instability region narrows with increasing conductance, indicating that the dc side conductance always contributes positively to the system damping. However, changes in the susceptance may strengthen or weaken the system depending on the actual susceptance value. Figure 4-7 shows the variation of the *SSF* with the susceptance. At high

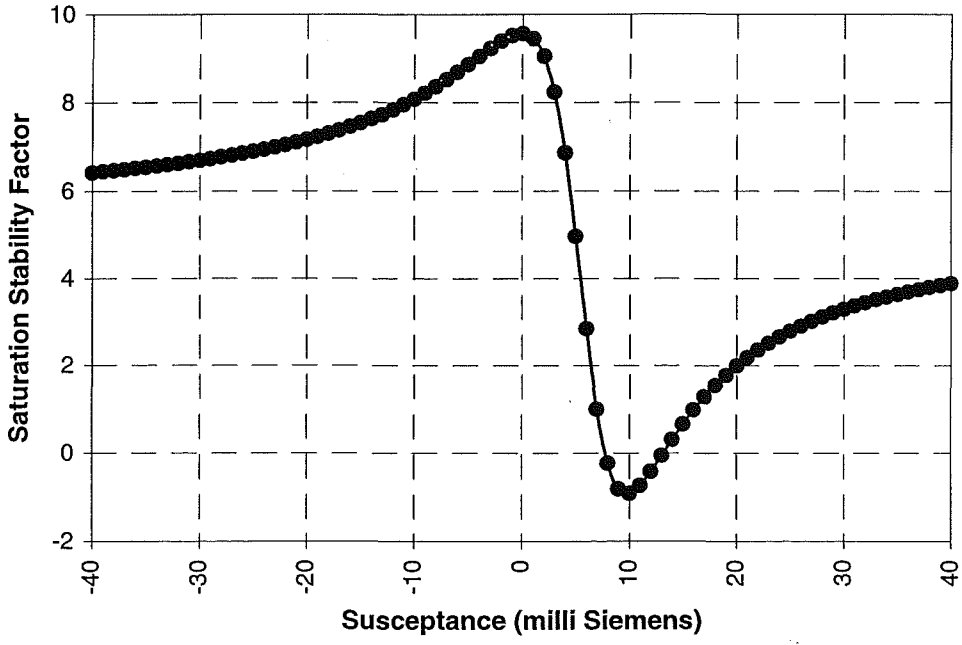


Figure 4-7: *SSF* versus dc side fundamental frequency susceptance

susceptance values (i.e. highly positive and highly negative values), the *SSF* has positive values, implying stable systems. Moreover, the closeness between the dots on the curve suggests the insensitiveness of the system stability to the change in the dc side susceptance except between 0 and +10 milli Siemens. Within this range, a small change in the dc side susceptance may drop the system *SSF* below zero and thereby expose the system to unstable conditions. Therefore, operation within this range of susceptance should be avoided to prevent the onset of core saturation instability.

4.2.4 Effect of the combined system impedance on the SSF

The studies above considers each of the impedances singly to evaluate their individual relationships with the *SSF* and the system stability. That analysis involves holding other impedances at their base case values while studying the effect from a particular impedance. The base case values have been deliberately tuned to result in highly unstable systems so as to highlight the effect of these impedances. Therefore, further analysis is required to evaluate whether each of the above relationships will still hold if one or more of the impedances deviate from the base case values. This section summarises the studies carried out on the combined effect of the system impedances, while full details are described in Appendix C.

The influence of R_{acn} on *SSF* is found to depend heavily on the characteristics of Z_{acp} and Z_{dch}. If the ac system is capacitive at the second harmonic frequency, the relationship between R_{acn} and the *SSF* reverses, that is higher values of R_{acn} improve the system stability instead of degrading it as in cases when the ac system is inductive (Figure C-2). This opposite effect is also observed if the dc side fundamental frequency impedance is inductive or less capacitive (Figure C-3). However, the *SSF* still tends to constant values as R_{acn} increases, indicating the diminishing effect of R_{acn} as it becomes higher, irrespective of the reactive properties of the other two impedances.

Conversely, the value of R_{acn} is observed to have moderate effect on the relationship between the system *SSF* and the characteristics of Z_{acp} and Z_{dch} (Figure C-6 and Figure C-11). Low R_{acn} lessens the impact from both Z_{acp} and Z_{dch} as the three dimensional *SSF* surface flattens to around the value of 1. On the other hand, the influence on *SSF* from Z_{acp} and Z_{dch} remains relatively unchanged when R_{acn} is high. However, lowering R_{acn} is observed to have shifted the *SSF* surface sufficiently to narrow the unstable Z_{acp} and Z_{dch} regions while raising it has widened the unstable regions (Figure C-7 and Figure C-12 compared to Figure 4-3 and Figure 4-6).

Furthermore, the reactive properties of Z_{acp} and Z_{dch} are observed to affect their respective relationships with the *SSF* (Figure C-8 and Figure C-13). When Z_{dch} is inductive, the *SSF* versus Z_{acp} surface reverses the trend shown when Z_{dch} is capacitive, with the smallest *SSF* value occurring within the positive susceptance half instead of the negative half (comparing Figure C-8i with Figure 4-2). Similarly, when Z_{acp} is made capacitive, the smallest *SSF* falls on the negative susceptance half of Z_{dch} instead of in the positive half when Z_{acp} is inductive (comparing Figure C-13i with Figure 4-5). However, making Z_{dch} slightly less capacitive is sufficient to remove the unstable Z_{acp} region (Figure C-8ii). On the other hand, making Z_{acp} slightly less inductive does not seems to have any impact on the unstable region of Z_{dch} (Figure C-13ii). This observation suggests that the system stability is more sensitive to the reactive characteristic of Z_{dch} than that of Z_{acp}.

In conclusion, the system impedances of R_{acn}, Z_{acp} and Z_{dch} are observed to significantly affect the system susceptibility to the convertor transformer core saturation instability. For the

instability to occur, the ac and dc networks connected to a rectification system must have the following combination of harmonic impedances:

- A low admittance at the fundamental frequency on the dc side with positive susceptance. This implies that the dc side is capacitive at the fundamental frequency with the presence of a series resonance near but slightly higher than the fundamental frequency.
- A low second harmonic admittance on the ac side with negative susceptance indicating an inductive ac side and the presence of a parallel resonance near but higher than the second harmonic frequency.
- A high resistance on the ac side near 0 Hz.

The system stability is highly dependent on the reactive characteristics of Z_{acp} or Z_{dch}, particularly when R_{acn} is high. Therefore, commissioning or decommissioning of reactive components can easily drive the system into unstable conditions. Similarly, changes in the operational routine may improve the system stability and may be sufficient to prevent the onset of the instability.

Finally, the effects of the system impedances on system stability, as deduced from the *SSF* technique described above, have been validated with dynamic simulations. The results of the simulations, described in the Appendix D, show close agreement between the *SSF* deductions and the time domain simulations.

4.3 Characteristics of convertor transformer

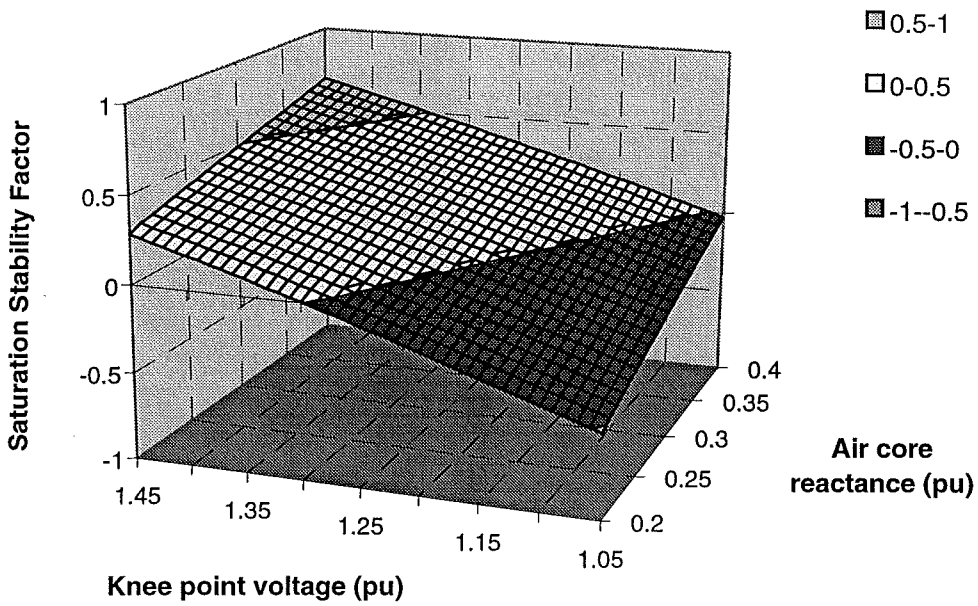


Figure 4-8: *SSF* versus convertor transformer magnetisation characteristic

One of the major contribution to the mechanism of this instability is the saturation effect of the convertor transformer. The chances of developing this instability is expected to be closely related to the transformer susceptibility to core saturation. This susceptibility is determined by

the magnetisation characteristics of the transformer, which is usually defined by the saturation knee point and the characteristic in the saturation region commonly referred to as the air core reactance. The transformer saturation contribution to the instability mechanism has been modelled with the I_{2+}:I_{0-} or X ratio (equation 3.9) described in the previous chapter. This ratio characterises the amount of positive sequence second harmonic current distortion being injected into the system from the transformer saturation which in turn is caused by the presence of negative sequence dc current emanated from the convertor. This ratio X is highly dependent on the transformer knee point and air core reactance, and was found to be realistically less than unity and approaching unity in the worst case. Several dynamic simulations were undertaken on the test case transformer with modified knee points and air core reactances to obtain the ratio X for different transformer magnetisation characteristics. The corresponding *SSF* was calculated and the results are plotted in Figure 4-8.

Low *SSF* is observed at low knee points and low air core reactances which correspond to near unity X ratio. This behaviour confirms the expectation that the system susceptibility to core saturation instability is closely related to the transformer susceptibility to core saturation and the amount of harmonic contribution when it is saturated.

4.4 Characteristics of convertor controller

All convertor controllers regardless of their characteristics, have several system parameters such as the ac voltage and the dc current as part of their inputs. Therefore, any distortion or modulation on these parameters will result in similar distortion and modulation on the control signals unless the controller has been specifically designed to filter out such distortions. However, it is impractical to account for all types of distortion and as a result, the control signals are usually being affected by it to a certain extent. The convertor controller acting on the distortion will reinject part of it back into the system through its actuator, which is usually the convertor firing angle. The behaviour of this reinjected distortion depends on the response of the controller. With a stabilising controller, the distortion is reinjected in such a way that it reduces the overall distortion. On the other hand, a destabilising controller will reinject the distortion so as to reinforce the original distortion and enhance the development of the instability.

In the convertor model used in the *SSF* formulation, the response of the convertor controller is embedded within the elements of the 3x3 harmonic interaction matrix (equation 3.2). In the derivation of this matrix, summarised in Appendix A, the convertor controller's effect is represented by the terms a_{19}, a_{20} and a_{21}. The first term a_{19} accounts for the transfer of any positive sequence second harmonic voltage distortion on the convertor ac side to the controller firing angle control signal; a_{20} translates any negative sequence dc voltage distortion on the ac side to the control signal while a_{21} reflects the modulation or distortion on the dc current onto the same control signal. Therefore, the responses of different convertor controllers can be easily incorporated into the analysis by defining these three terms. For a typical constant current controller, both a_{19} and a_{20} are zero and a_{21} is defined by the frequency response of the proportional and integral transfer function at the fundamental frequency, including the first order lag response of the current transducer.

The *SSF* approach greatly reduces the effort required to study the effect of the convertor controller on the system susceptibility to core saturation instability. For any controller, the three aforementioned terms are reevaluated and the corresponding *SSF* is recalculated. Changes in the *SSF* depict the relative stability of each controller configuration. Figure 4-9 shows the simplified block diagram of a constant current controller customarily used at the

rectifier. The response of the controller loop including the measuring transducer is simplified to the control gain magnitude (G) and the control phase angle (P). The corresponding *SSF* of the test system for a range of gain magnitude and phase responses of this control loop is shown in Figure 4-10.

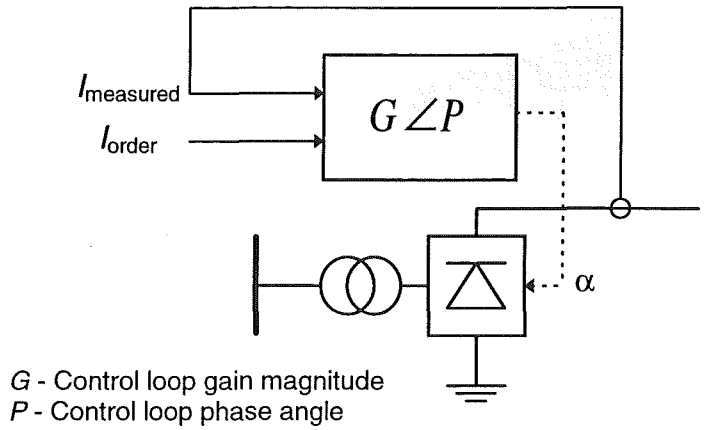


Figure 4-9: Block diagram of a general constant current controller

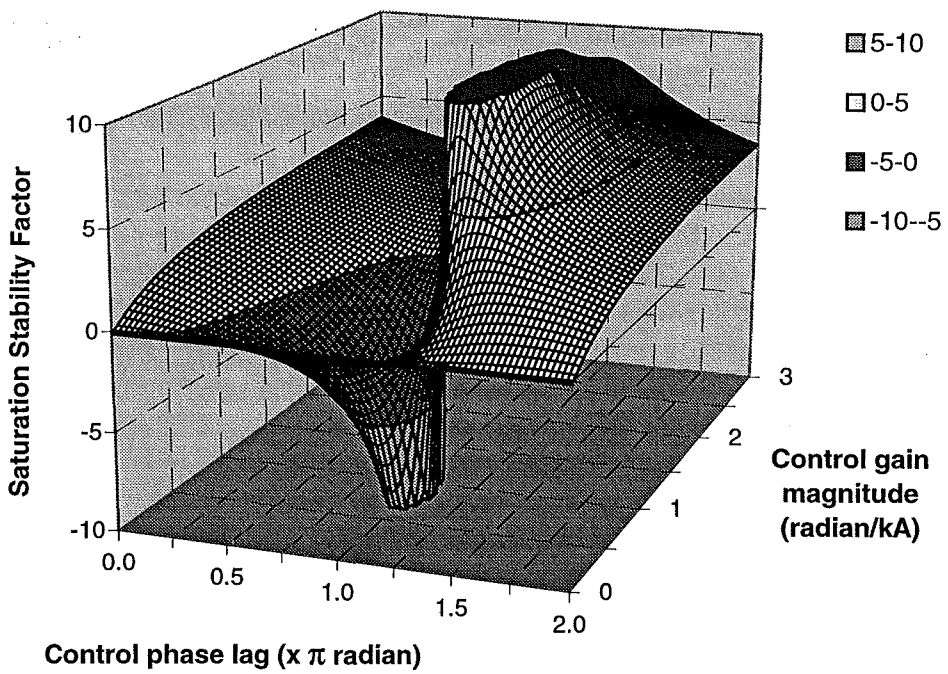


Figure 4-10: *SSF* versus frequency response of a constant current controller

The variations in *SSF* for the range of responses shown above clearly highlight the dependence of the system stability on the convertor controller. A positive *SSF* indicates that for this test system, the constant current controller is mostly stable except when its control gain magnitude is small and the phase response is about 0.8π radian lagging. These unstable responses are summarised in Figure 4-11 which shows that the test system is unstable without a convertor controller (i.e. when the control magnitude gain is zero) and when the phase

response is between 0.75π and 1.75π radians. The stability of the system improves with the control gain magnitude.

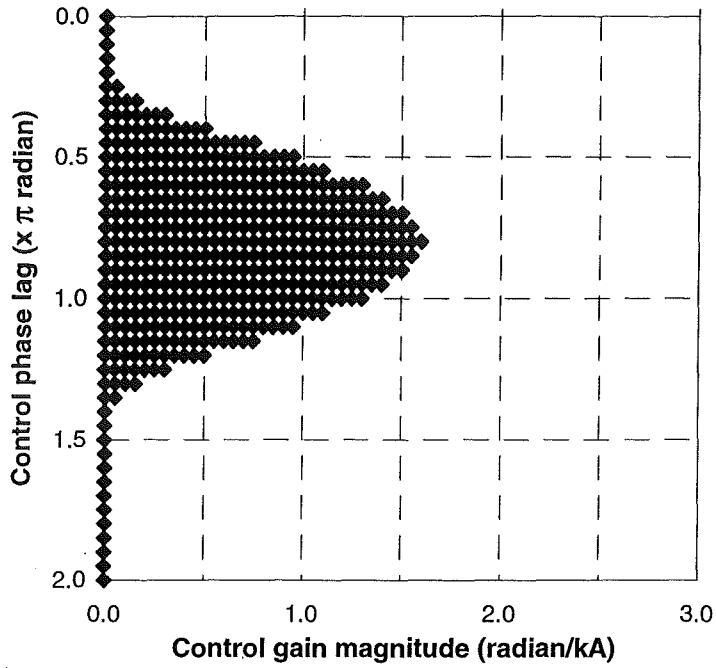


Figure 4-11: Range of constant current controller responses with negative *SSF*

Furthermore, Figure 4-10 shows that around the gain magnitude of 1.0 kA/radian and phase angle of 0.8π radian, the control responses with highly positive *SSF* are very close to those with highly negative *SSF*. This close proximity between highly stable and unstable conditions suggests that the system susceptibility to the instability is immensely sensitive to the controller responses. A minor change in the controller response may be sufficient to precipitate this type of instability. On the other hand, this also indicates the possibility of countering the instability by proper tuning of the frequency response of the convertor controller. However, this promising opportunity is complicated by the fact that the impedances of the HVDC system are constantly varying and the controller's behaviour toward the development of the instability changes with the impedances. This interdependency is highlighted with an illustration described in Appendix E and summarised below.

Figure 4-12 shows the unstable control responses for two similar HVDC systems except for a minor difference in the ac side second harmonic susceptance. There are four regions in the figure, each corresponding to a different combination of stability of the test systems. Controllers in region A exhibit stabilising effect in both systems while those in B are destabilising. Those in C are only suitable for system 1 while those in D are useful for system 2 only. This simple illustration highlights the vast differences in the effect of the convertor controller on almost identical systems. It shows the fragile relationship between the convertor controller and the system core saturation stability when the system impedances are expected to vary. This leads to the conclusion that it is impossible to construct a common controller which is capable of preventing the development of this instability for all variants of HVDC systems. On the contrary, a stable controller under one installation may become highly destabilising when introduced to another scheme. This further enhances the need to undertake independent analysis for different systems and the resultant controllers are most likely to

possess different characteristics. This illustration has been validated with dynamic simulations and the results are described in Appendix E.

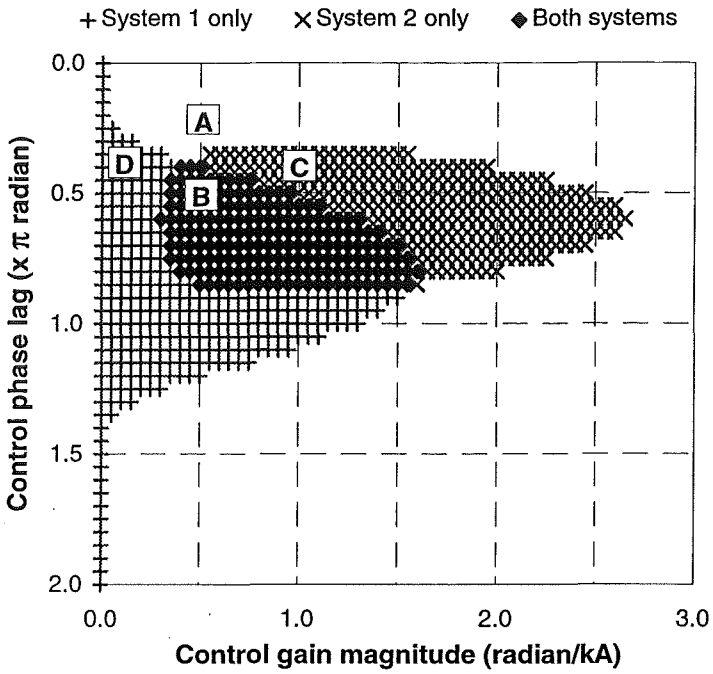


Figure 4-12: Unstable control responses for two different systems

4.5 Effect of convertor steady state operating parameters

The main function of a HVDC system is to transfer the required amount of power from one end of the line to another. This is usually achieved by controlling the convertor firing angle, the dc current and to a lesser extent the ac and dc voltages. The voltages are usually kept high to reduce the amount of resistive losses through the link. Therefore, the ac and dc side voltages are assumed to be kept constant in the following analysis.

The transfer of harmonics between the ac and dc sides of a HVDC convertor depends on the steady state operating parameters of the convertor. The convertor harmonic interaction matrix of equation 3.2 is derived from these steady state parameters as outlined in Chapter 3 and Appendix A. Changes to these parameters will alter the harmonic interaction and in turn affect the system stability. This direct frequency domain convertor model facilitates the evaluation of the effect of each of the steady state parameters as it allows individual parameters to be altered independently. The corresponding changes to the *SSF* depict the effect of the altered parameter. In this section, the effects of operating the convertor at different firing angles, commutation angles and dc currents are evaluated.

Changes to the convertor firing angle not only affect the magnitude of the transferred harmonics but also the phase shift introduced. Figure 4-13 shows the variation of *SSF* with convertor firing angle. The figure shows an approximately linear inverse relationship between the *SSF* and the firing angle. This implies that the likelihood of developing core saturation instability increases when the convertor is operated at high firing angle. Fortunately, the firing angle is normally kept low around 15° at the rectifier so as to minimise the reactive

consumption by the link, while maintaining a safe margin to prevent misfires of the valves. This common practice has assisted in minimising the risk of developing core saturation instability.

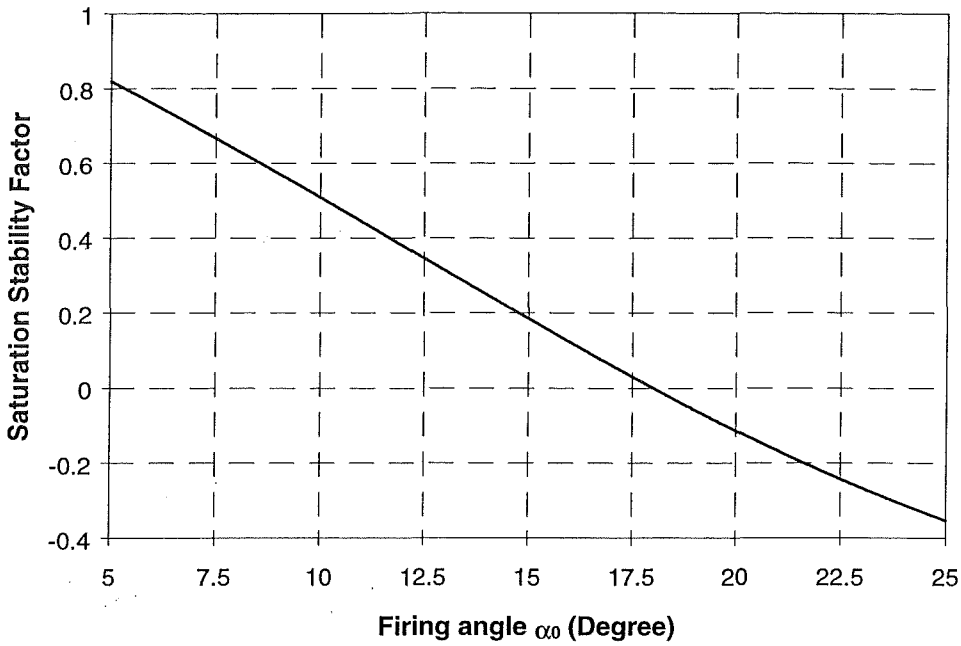


Figure 4-13: *SSF* versus convertor firing angle

The variation of the convertor commutation period is known to introduce an apparent resistance which helps to damp oscillations on the convertor dc side [Bahrman *et al.*, 1986]. At low harmonic orders, this apparent damping is found to be directly proportional to the duration of the commutation process. Figure 4-14 shows the *SSF* plotted against the commutation period assuming other parameters including the firing angle remain unchanged. It is obvious that the system stability improves with the length of the commutation period. The *SSF* increases with the commutation angle until 20° where the *SSF* curve levels off to a constant value. Moreover, the variation of *SSF* with commutation angle, shown in Figure 4-14, is larger that that of the convertor firing angle shown in Figure 4-13. This improvement in system stability with the commutation period conforms with the additional apparent damping obtained from longer commutation duration and emphasises the importance of this apparent damping to the system stability.

In Figure 4-13, the commutation angle is assumed to be unaffected by changes in the firing angle. Figure 4-15 shows the corresponding *SSF* curve if the variation of commutation angle is taken into consideration. Clearly, the reduction in the commutation period with the increase in firing angle reduces the system *SSF* to a greater extent. Besides the influence of the convertor firing angle, the commutation period is also affected by the dc current and the commutating reactance. As the commutation period is directly proportional to these parameters, the system stability and *SSF* will also be directly dependent on them. Maintaining the firing angle small during heavy dc loading will keep the commutation period long and as a result minimise the system susceptibility to core saturation instability. Moreover, a transformer with larger leakage reactance will also improve the system stability.

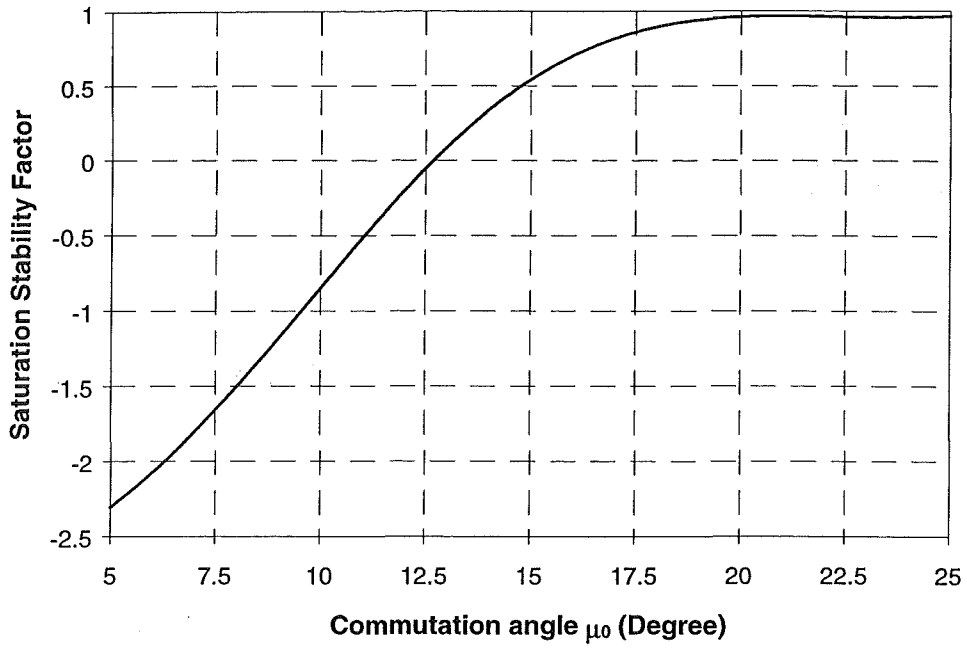


Figure 4-14: *SSF* versus convertor commutation angle

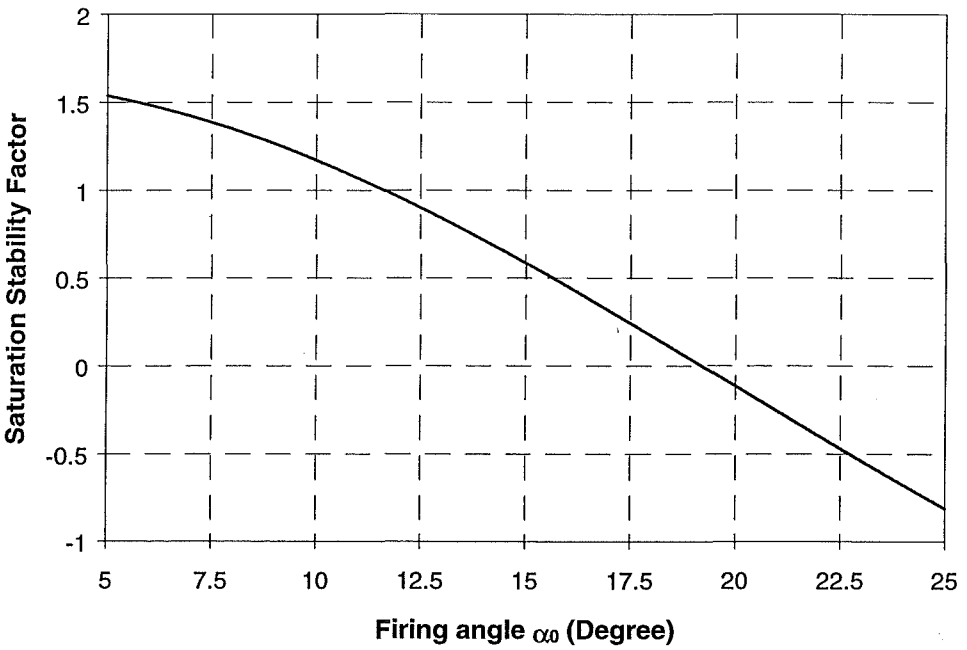


Figure 4-15: *SSF* versus convertor firing angle with consideration of consequential change to commutation angle

This study has shown that the influence of the steady state operation parameters of the HVDC convertor on the system susceptibility to the development of core saturation instability. Therefore, by proper tuning of the steady state operating parameters, it may be possible to prevent the development of such instability. However, besides the susceptibility to the core

saturation instability, other constraints or requirements placed on the system have to be considered when deciding on such parameters. Nonetheless, for this particular rectifier system operating with constant firing angle (ie. without convertor controller), the system is more likely to develop this type of instability when it has high firing angle and low commutation period, which is possible under light dc loading. Figure 4-16 shows that the *SSF* and hence the system stability improves with the dc current, which directly reflects the dc loading level assuming that other parameters, including the firing angle and the commutation voltage remain constant. However, the influence from the convertor controller may overturn these responses causing the degradation of the system stability at high dc loading [Ainsworth, 1977].

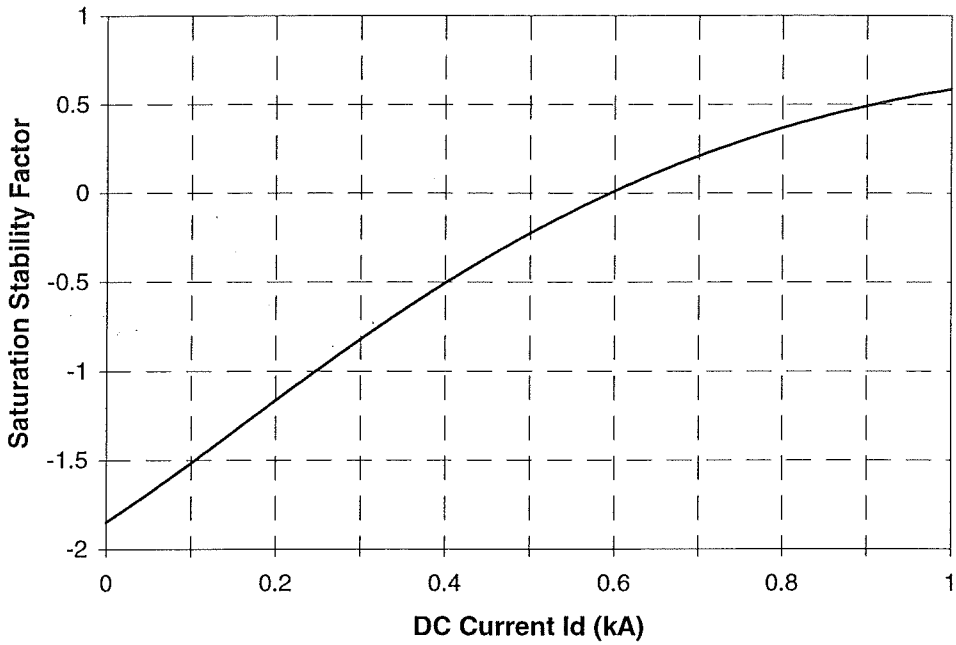


Figure 4-16: *SSF* versus dc current

4.6 Stability at the invertor

All of the cases described above have been carried out assuming the convertor operating in the rectification mode. In this section, the characteristics of core saturation instability are reanalysed considering the convertor operating as an invertor. While the transfer of harmonics through the invertor is expected to be comparable to that of the rectifier, the strong dependency of the instability on the operating parameters, as shown above, may significantly alter the instability characteristics at the invertor end.

Figures 4-17, 4-18 and 4-19 show the variation of *SSF* with the harmonic impedances of the invertor ac and dc sides. The *SSF* still decreases with the R_{acn}, indicating that the effect of R_{acn} on the transformer saturation remains the same at both the rectifier and invertor. Higher R_{acn} will cause most of the negative sequence dc current to flow into the transformer magnetising inductance thus raising the level of transformer saturation, and thereby increasing the system susceptibility to the instability. On the other hand, the variation of *SSF* with Z_{acp} and Z_{dch} at the invertor appears to be different compared to those at the rectifier. The peaks and troughs

of the *SSF* surfaces are observed to occur on opposite side of the susceptance compared to those at the rectifier. Figure 4-18 shows that the second harmonic admittance at an unstable invertor has low conductances and positive susceptances. This means that Z_{acp} is capacitive at this frequency which is different to that at the rectifier, where Z_{acp} is expected to be inductive. Although a parallel resonance should still exist near the second harmonic frequency, at the invertor, the resonance frequency is lower than the second harmonic frequency whereas it is higher at the rectifier. A similar sort of deviation is observed for Z_{dch}, the dc side impedance at the fundamental frequency. At the rectifier, this impedance is capacitive in an unstable system, whereas at the invertor it is inductive. Moreover, the susceptance at the invertor end with negative *SSF* spreads over a much wider range compared to that at the rectifier. However, the conductances at both ends are low, implying the presence of a series resonance at the dc side near the fundamental frequency. At the invertor, the resonance frequency will be lower than the fundamental frequency whereas that at the rectifier will be higher.

Besides the differences in the reactive characteristics of the impedances at the rectifier and invertor ends, the different responses of the controllers used at both ends of the link will also affect the system stability differently. Invertors are usually designed with several modes of operation, each with its own control characteristics. All these responses have to be analysed to assess the system stability under each operating condition. Similarly to the response at the rectifier, the system stability at the invertor is found to be highly dependent on the frequency response of the controller.

The commutation duration at the invertor end also introduces apparent damping to the dc side. Therefore, raising the invertor firing angle will lengthen the commutation period and in turn raise the apparent damping and stabilise the system. However, the need for a sufficient extinction angle in order to prevent commutation failure may cause the invertor system to become susceptible to the instability.

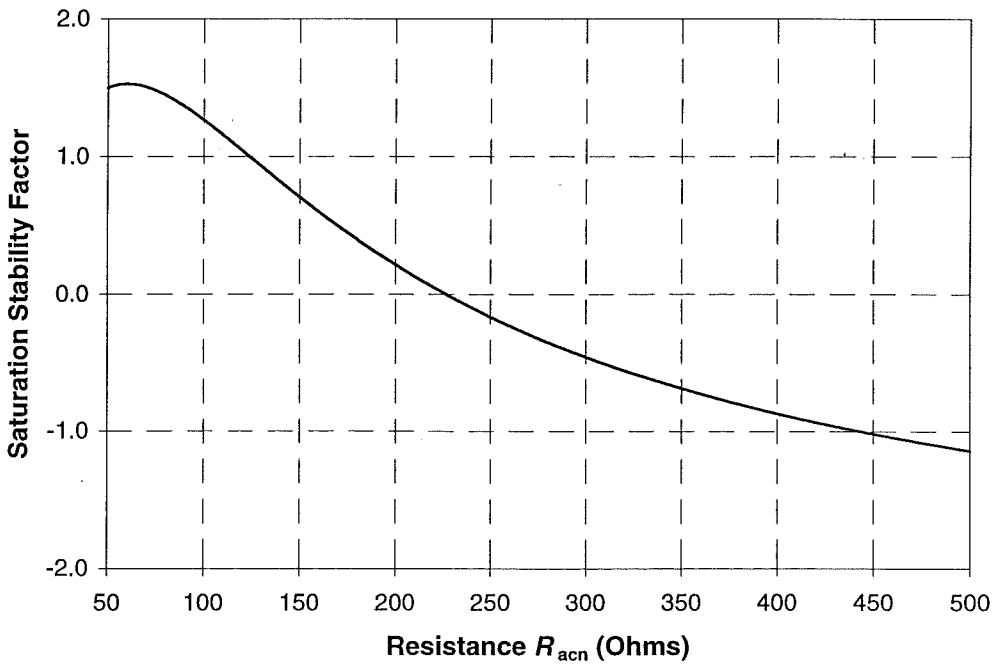


Figure 4-17: *SSF* versus R_{acn} at the invertor

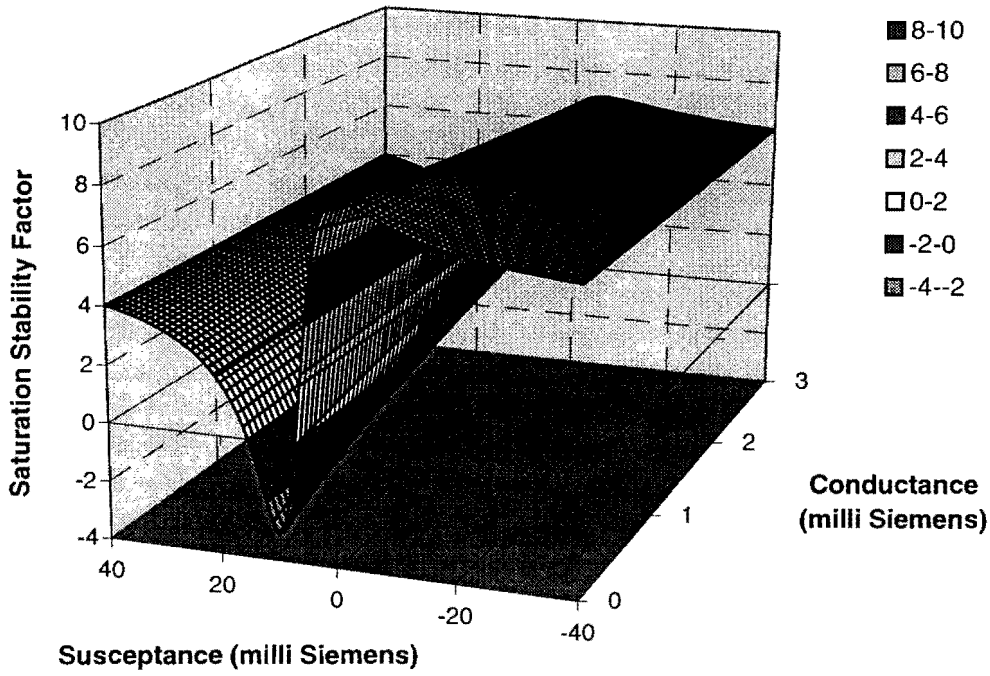


Figure 4-18: *SSF* versus Z_{acp} at the invertor

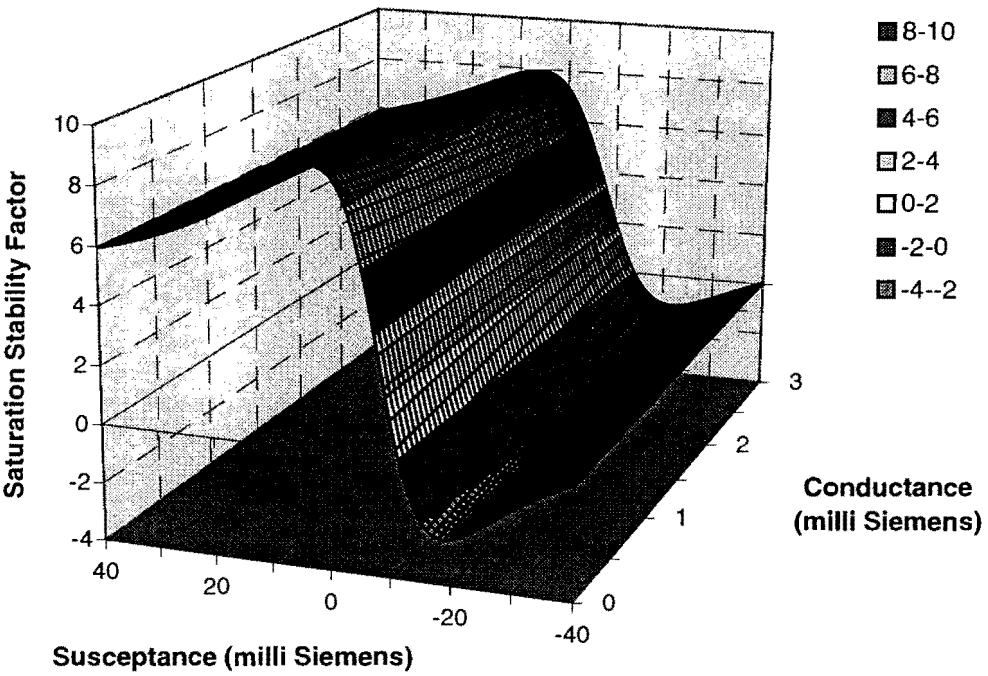


Figure 4-19: *SSF* versus Z_{dch} at the invertor

4.7 Stability at back-to-back intertie

In the analysis described above, the remote end station is assumed to be a simple constant current or voltage source and therefore, the effect of the remote end convertor and ac network have not been accounted for. This is a reasonable approximation for HVDC schemes with

long dc transmission lines where the dc side impedance at the fundamental frequency is primarily made up of the impedance of the dc line including the smoothing reactor and the harmonic filters, provided there is no special tune circuit on the dc transmission system. However in back-to-back schemes and particularly those without smoothing reactor, there is a close electrical coupling between the two convertors and the interconnected ac systems, and hence they will affect each other's response to the instability.

The effect of the convertor at the opposite end of the link can be incorporated into the *SSF* analysis by representing the convertor as an equivalent impedance at the fundamental frequency. Wood has derived the formulation to calculate the dc side impedance of a convertor from the harmonic impedances of the connected ac system. This formulation is included in Appendix A. Ignoring the transformer saturation effect and assuming that the convertor is operating at constant firing angle, the convertor dc side equivalent impedance will have a similar reactive characteristic as that of the ac side second harmonic impedance. Therefore, an inductive invertor ac system will cause the dc side fundamental frequency impedance looking from the rectifier dc terminal to appear inductive and thereby avoids the onset of the instability at the rectifier. Likewise, a capacitive rectifier ac system will help to stabilise the invertor system by making its dc side impedance capacitive at the fundamental frequency. Moreover, any resistance near 0 Hz or at the second harmonic on the ac side will be reflected as further resistance on the dc side thus helping to stabilise the remote system.

The use of HVDC back-to-back interties to interconnect large ac networks has been widely accepted as a useful way of maintaining steady power flow between the ac networks. Although these schemes provide more controllability compared to the ac interconnections, the connected ac networks are usually relatively weak, resulting in low order resonances at the convertor terminals and making them prone to the core saturation instability. However with comparable ac network sizes at both the rectifier and invertor ends, the core saturation instability is most likely to occur only at one end of the scheme. This is due to the opposite reactive requirements of the impedance for an instability to occur at the rectifier and invertor ends as outlined above. Moreover, the high resistance at the unstable end will be reflected onto the dc side as additional damping which will tends to stabilise the other system. These deductions are only valid provided the response of the convertor controller does not drastically alter the aforementioned reactive requirements of the impedance for the instability and the effect of local transformer saturation to the remote end stability is ignored.

In a back-to-back intertie, a convertor controller not only affects the stability at the local end of the scheme, also the amount of damping (either positive or negative) on the dc side as seen from the other convertor. Therefore, a stabilising controller at the local end of the system may cause the system at the other end to become unstable. On the other hand, it is also possible for the remote end controller to exhibit a stabilising effect on the local system. Figure 4-20 shows the effect of the rectifier constant current controller on the stability of the invertor system. The rectifier equivalent dc side impedance is calculated for a wide range of control gain magnitude and phase responses and is applied to the *SSF* formulation at the invertor. The figure shows substantial variations in the *SSF* indicating the strong effect the rectifier controller has on the stability of the invertor system. This observation emphasises the need to consider the consequential impact on the stability of the remote end system when undertaking any modification at the local end.

Figure 4-21 shows the range of magnitude and phase responses of the rectifier controller which will be destabilising for the invertor. Comparing this figure with that in Figure 4-11, showing the unstable controller responses for the rectifier local system, it is observed that

there are some overlaps between the two regions. This implies that some control responses will cause both the rectifier and invertor systems to become unstable. On the other hand, it also indicates the possibility of using the opposite end convertor controller to stabilise the local system. This is particularly attractive when some constraints have prevented the needed modifications on the local system to counter the instability. Moreover, with close proximity between the convertors, a unified controller may be a more effective solution.

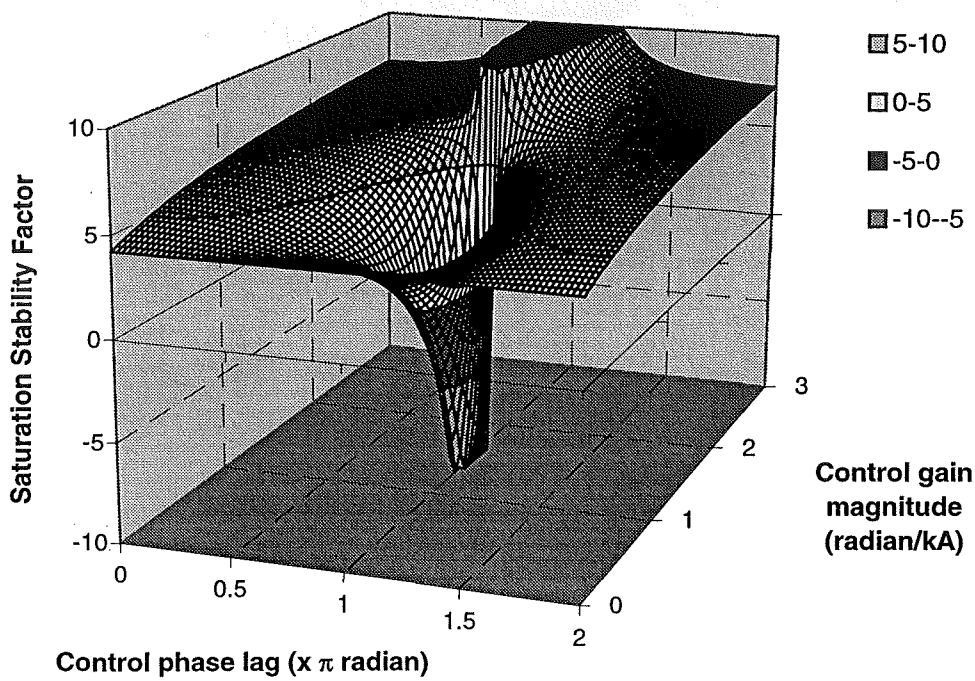


Figure 4-20: Invertor *SSF* versus rectifier controller magnitude and phase responses

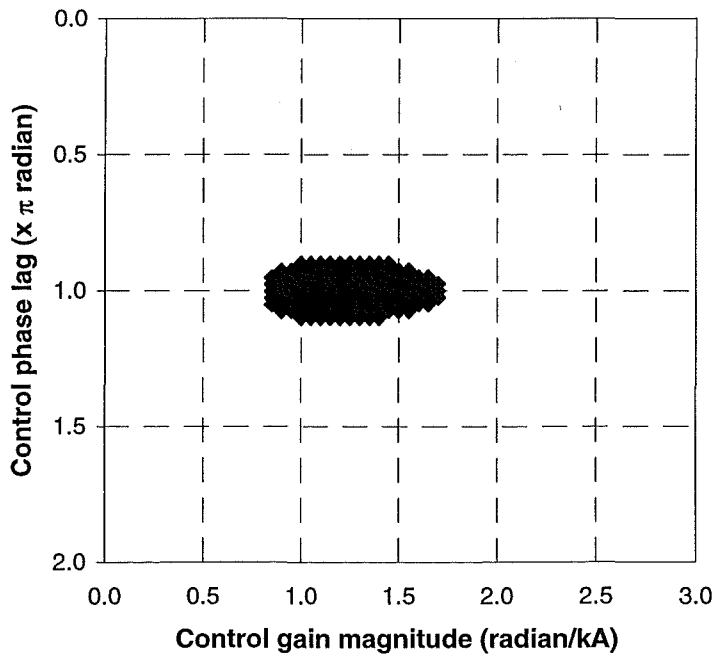


Figure 4-21: Range of rectifier controller responses resulting in negative invertor *SSF*

4.8 Conclusion

The analysis described in this chapter has revealed the characteristics of the impedances on the ac and dc sides of an unstable convertor. It has been shown that a rectifier system prone to core saturation instability has the following combination of harmonic impedances:

- A low and predominantly capacitive dc side impedance at the fundamental frequency with the presence of a series resonance near but higher than the fundamental frequency.
- A high and predominantly inductive ac side impedance at the second harmonic frequency with the presence of a parallel resonance near but higher than the second harmonic frequency.
- A high ac side resistance near 0 Hz.

Conversely, an unstable invertor system will have a predominantly inductive dc side impedance and a predominantly capacitive ac side impedance. High ac side resistance near 0 Hz will also enhances the instability at the invertor end. Even though these characteristics are derived without considering the effect of the convertor controller, the generally low control gain magnitude means that these patterns are still expected in unstable systems. The information generated from these studies is valuable in the design of harmonic filters to prevent the onset of the instability. It can also be used to reveal unstable conditions which should be avoided unless control measures are taken to damp the instability.

The stringent requirement on the impedance profiles of a HVDC system for the instability to develop implies that this sort of instability should be a rarity if the convertor controller contribution is small. However, this instability has been reported at all variants of HVDC schemes under different conditions. This suggests that the development of this harmonic instability always involves a destabilising contribution from the convertor controller. Therefore it should be possible to prevent the development of this instability by modifying the existing control parameters or by introducing auxiliary controls. Moreover the influence of the controller has been shown to vary widely under different conditions and therefore it is essential to carry out separate analysis on different systems or for different operating conditions in the same system. In Chapter 5, the *SSF* technique is utilised to determine possible control solutions for this instability.

The apparent resistance on the convertor dc side resulting from the convertor commutation process has been shown to stabilise the system by providing additional damping of the oscillations. This additional damping is directly proportional to the length of the commutation process and therefore longer commutation angle have been shown to raise the system *SSF* and hence improve the stability. Besides that, the stability at the rectifier system has been shown to improve when the firing angle is reduced. Reducing the rectifier firing angle not only raises the *SSF* by its own accord, but also lengthens the commutation, resulting in greater apparent damping. On the other hand, the stability at the invertor system improves when the firing angle is increased which also causes the commutation process to become longer raising the apparent damping.

In the back-to-back scheme, the stability at one station will be affected by the characteristics of the remote end convertor and the properties of the connected ac networks. Unfavourable conditions at one end of the link are most likely to show stabilising effect on the remote end convertor system. Therefore core saturation instability is expected to cause problems only at one end of a back-to-back system. However, it is still possible for instability to occur at both ends of the link if one or both of the convertor controllers are destabilising. The analysis has

highlighted the need to consider the stability at both ends of the back-to-back scheme when determining control solutions.

Lastly, the likelihood of a system developing this instability has been shown to be closely related to the transformer susceptibility to core saturation. Transformers with low knee point voltages will be easily saturated by relatively low dc current, while those with low air core reactance cause more substantial distortions when saturated. Lowering of both of these parameters reduce the *SSF*, degrading the system stability.

The *SSF* approach has been successfully used to reveal the characteristics of HVDC systems which are susceptible to core saturation instability. The analysis has considered the effect of ac and dc side impedances, the magnetisation characteristics of the convertor transformer, the frequency responses of the convertor controller and the way the convertor is being operated in the steady state. The onset of core saturation instability has been shown to be strongly dependent on all of these parameters. Therefore, the investigation for control solutions to be described in Chapter 5 will have to take all of them into consideration.

Chapter 5

Solutions for core saturation instability

5.1 Introduction

The control and prevention of the convertor transformer core saturation instability is the ultimate aim of any such analysis on the subject. The evaluation of the *SSF* has largely indicated that this instability can be prevented by operating the system away from the unstable conditions. This type of actions may involve modification to the system impedances, tuning of the convertor controller parameters or the convertor steady state operating parameters. Although the purpose of the changes to these parameters is to modify the system response at the frequencies related to this instability, it usually affects the system response at other frequencies as well. The design of such preventative measures has to ensure that other system requirements or constraints are still met after the modifications. These actions can be broadly regarded as passive measures.

On the other hand, active measures can be applied to stabilise the system when the development of the instability is detected. This type of solution has been used to prevent core saturation instability in existing schemes, with some sensing instruments estimating the level of transformer saturation and appropriate action taken in accordance with the extent of the saturation. Active measures should be designed to function at certain limited range of frequencies without altering the system response significantly under normal operating conditions. This will allow the system to be operated as usual, but with the added security of some stabilising action when the instability is suspected.

The problem of harmonic instability can generally be solved by providing sufficient damping at the relevant frequencies. In particular, the development of the core saturation instability can be controlled or suppressed if there is sufficient damping at the fundamental frequency on the dc side or at the positive sequence second harmonic in the ac system. It can be achieved either in the form of system damping or as apparent damping provided through the convertor controller. In all the existing HVDC schemes with reported cases of this instability, the problem has been solved by introducing certain modulations to the convertor controller parameters.

Due to the great differences in the characteristics of the various HVDC systems, it is difficult to pinpoint which is the best solution to counter this instability. The high dependency of the system stability on the properties of HVDC scheme, as outlined in previous chapters, suggests that the most appropriate solution for one system will not suit the others. This chapter does not attempt to establish the best control or preventative measure, but to demonstrate the value of the *SSF* technique in the determination of possible control solutions. Modifications to the system impedances or changes to the system operating parameters, either in passive or active form, are derived using the *SSF* approach and the results are illustrated with the help of PSCAD/EMTDC dynamic simulations.

The CIGRE HVDC benchmark model, used as the test case, is briefly introduced in the next section, with particular emphasis on the parameters concerning this type of instability. Modifications are made to the system in order to enhance the development of the instability. This is followed by an illustration of possible stabilising techniques, including the conventional method of ac harmonic filters and the modifications commonly applied to the convertor controller. Lastly, the benefit of using an auxiliary convertor controller with a control loop incorporating a high pass filter is demonstrated.

5.2 Description of test system

The analysis of HVDC system has in the past been hampered by the lack of a standard test system allowing the comparison of different control proposals or modeling techniques on a common basis. The Working Group 14-02 (Controls in HVDC Systems) of CIGRE Study Committee 14 (DC Links) decided to establish a standard AC/DC system to alleviate this problem, and the first benchmark system was published in 1991 [Szechtman *et al.*, 1991]. This model since then has gained wide acceptance among researchers and has been included as reference in a growing number of international publications [Szechtman, 1993].

Figure 5-1 shows the schematic diagram of the benchmark model. The system configuration is rather simple but is purposely designed to be operationally difficult. It consists of a two-terminal HVDC scheme with the ac networks represented by Thevenin equivalent circuits. Two banks of damped harmonic filters, tuned to low and high frequencies respectively are provided at each convertor terminal and capacitor banks are added to fulfill the reactive requirements. The DC link with a rather high capacitance and relatively low inductance is typical of a medium or long cable system. The SCR (Short Circuit Ratio) of the rectifier and invertor systems is deliberately made low at 2.5, and with a rather high admittance angle of 84° at the rectifier. The high angle is used to represent the predominantly generating system at the rectifier, resulting in rather poor damping. In addition to the weak ac systems, the dc side is tuned to resonate near the fundamental frequency, which is in complement with the second harmonic resonance in the ac systems, making the benchmark system highly demanding to operate and presenting a difficult case for new control techniques or strategies.

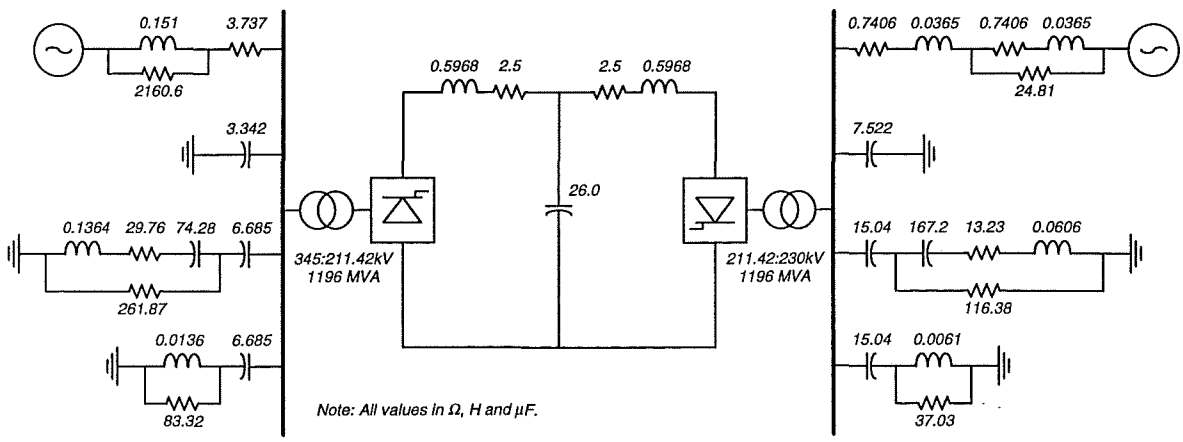


Figure 5-1: Schematic diagram of CIGRE first HVDC benchmark model

Although the model is designed to be operational difficult, with resonance in both the ac and dc systems, it was found to be rigid against core saturation instability. Figure 5-2 shows the frequency response of this test system. The rectifier ac system impedance is found to be capacitive at the second harmonic which does not meet the prerequisite for the development of the instability. Although the dc side is capacitive at the fundamental frequency, the capacitance is too low for the instability to occur. Moreover, the low susceptibility of the convertor transformer to core saturation further enhances the system stability. The low firing angle around 15° with a rather long commutation period provides a substantial apparent damping on the convertor dc side and contributes to the system stability. The benchmark system was therefore modified to illustrate the build up of the instability and to demonstrate the application of the *SSF* approach to derive control and preventative measures.

The illustrations in this chapter consider the system stability only at the rectifier end. The invertor system was not modified and with the dc cable system between the convertors, the invertor is assumed to have negligible effect on the stability of the rectifier system. The

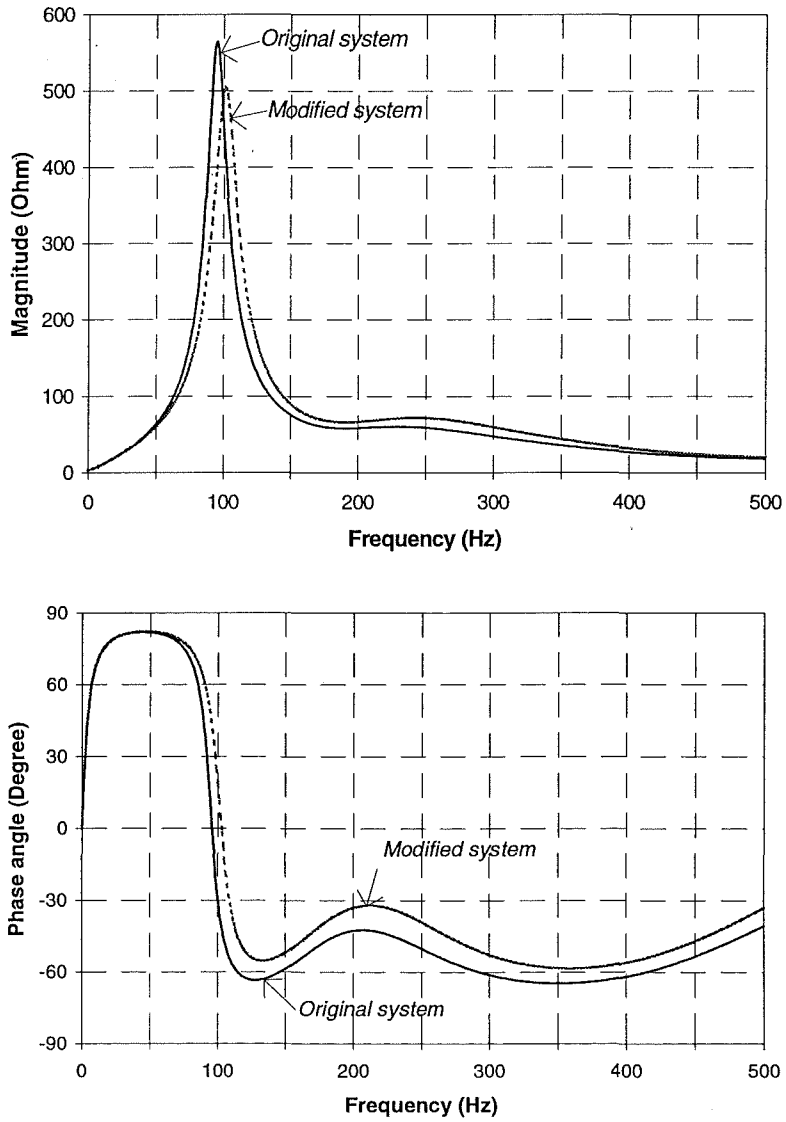


Figure 5-2: Frequency response of CIGRE HVDC benchmark model

following modifications were made on the rectifier end of the benchmark model to enhance the development of the core saturation instability,

- The dc link is added with a second identical cable system, including the smoothing reactor, in parallel. This halves the overall line resistance and inductance while doubles the line capacitance.
- The ac side second harmonic impedance is made inductive by reducing the capacitance of the compensation capacitors. The capacitance of 3.342μF is reduced to 0.6684μF, thus changing the second harmonic impedance from 399.61-j223.20Ω capacitive to 474.98+j153.02Ω inductive. This change has shifted the ac side resonance frequency from about 96Hz to 103Hz, a value just over the second harmonic. Despite these modifications, the frequency response of the rectifier ac system remains relatively unchanged as shown in Figure 5-2, and has no significant impact on the system response at other frequencies.
- The ac voltage source is raised from 1.07 p.u. to 1.10 p.u. This is carried out to compensate for the reduction of reactive power supply at the convertor and to deliberately increase the convertor firing angle from 15° to 20°.
- Increasing the convertor firing angle has the consequential effect of reducing the commutation period. Both effects have the tendency to destabilise the system.
- The convertor transformer knee point and air core reactance are lowered, from 1.22 p.u. and 0.36 p.u. to 1.10 p.u. and 0.20 p.u. respectively, to achieve a highly susceptible transformer. The transformer leakage reactance is also lowered, from 0.18 p.u. to 0.12 p.u. to further shorten the commutation period and hence reduce the amount of apparent damping on the system. The increase in the convertor firing angle and the reduction in the transformer leakage inductance has reduced the commutation angle from approximately 22.87° to 19.84°.
- The integral time constant of the constant current PI controller at the rectifier is reduced from 0.0091 to 0.0030 second, but a small change is made to the proportional gain from 1.0989 to 1.0607 radian/per unit dc current.

The combination of changes made to the system configuration and control, as outlined above, has brought about the development of the kick-started type of core saturation instability. The *SSF* of the system alters from a positive value of 0.074 to a negative value of -0.152. This unstable test case was simulated in PSCAD/EMTDC and the results, shown in Figure 5-3, depict the build up of the instability.

The simulation was carried out in a similar manner to other simulations described in the preceding chapters, i.e. it was run to steady state (reached at about 1 second) and then a firing angle modulation was introduced. The external stimulus was maintained for 0.5 seconds and assessment of the system stability was based on its ability to settle back to pre-disturbance conditions after 1.5 second. The continued build up of distortion on the dc current and the persistent increase in the level of the saturating dc component in the transformer magnetising current (I_{mag}) confirm the presence of the convertor transformer core saturation instability. Although several aspects of this unstable system are somewhat unrealistic, it is useful for demonstrating the use of *SSF* in the design of control solutions.

5.3 Possible solutions

The design of appropriate control measures for this instability has been heavily dependent on the experience of the engineer. In most occasions, several trials are required before reaching a satisfactory solution. Moreover, the effectiveness of each measure can only be determined

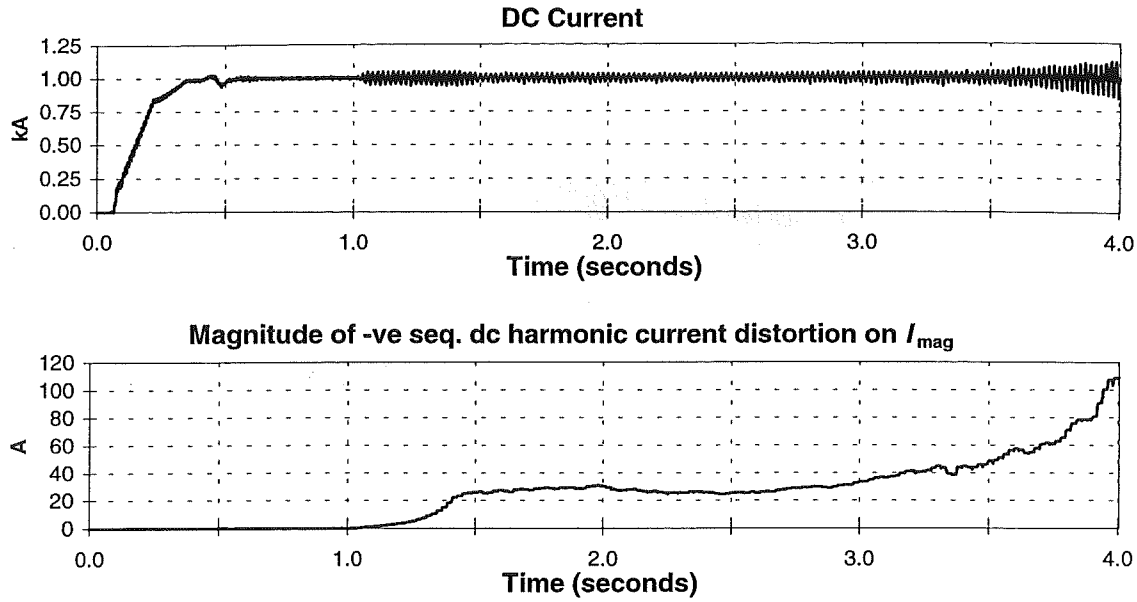


Figure 5-3: Simulation results of test system with instability (base case)

through trials or experiments, either in the field or through simulators. Despite the success of these measures in countering the instability, there is no clear indication that the implemented actions are the most effective and appropriate ones.

On the other hand, differences in the value of *SSF* show the relative stability of one scheme compared to another. This enables the effectiveness of the control measures to be compared by analysing the resultant *SSF* of each scheme. Furthermore, the *SSF* approach can be used to derive the most appropriate parameter values for a particular control action. Several possible control measures are described in the following sections and the *SSF* approach is used to determine the values of their parameters or components.

5.3.1 Modification of the system

It has been shown in the previous chapter that core saturation instability will only occur under certain combinations of impedances on both sides of the convertor. Therefore, this instability can be alleviated or eliminated by undertaking modifications to the system to avoid the unstable regions. An ac filter tuned to the second harmonic has been installed in the Chateauguay scheme to stabilise the system at this frequency under all operating conditions [Hammad, 1992]. By means of such a filter, the ac system impedance is significantly reduced with sufficient damping around the second harmonic, eliminating the corresponding instability encountered in the scheme.

A stabilising harmonic filter can be constructed from the range of admittance with positive *SSF*. For this demonstration, the filter admittance is chosen to be 1.0 + j 10.0 milli Siemens, resulting in a RLC filter configuration of 9.9Ω, 0.6002H and 3.3425μF. The resonance frequency of the harmonic filter is tuned to around 112Hz and the resultant *SSF* of the system with the filter has a positive value of 0.236. The results of the simulation of the test system with the harmonic filter are shown in Figure 5-5, clearly depicting the stability of the system. The convertor transformer is subjected to similar level of saturating dc current as the base case. However, the distortion on the dc current and the level of saturating dc current decay

away as soon as the firing angle modulation is removed. This filter configuration is chosen for demonstration purpose only and has not been optimised for normal operation.

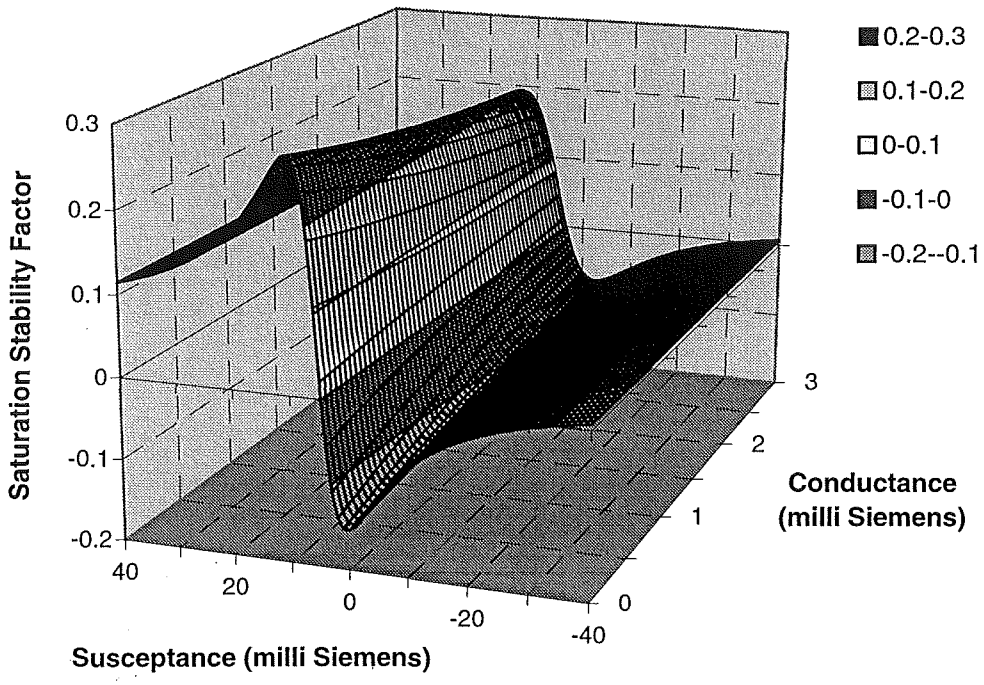


Figure 5-4: *SSF* versus second harmonic admittance of ac harmonic filter

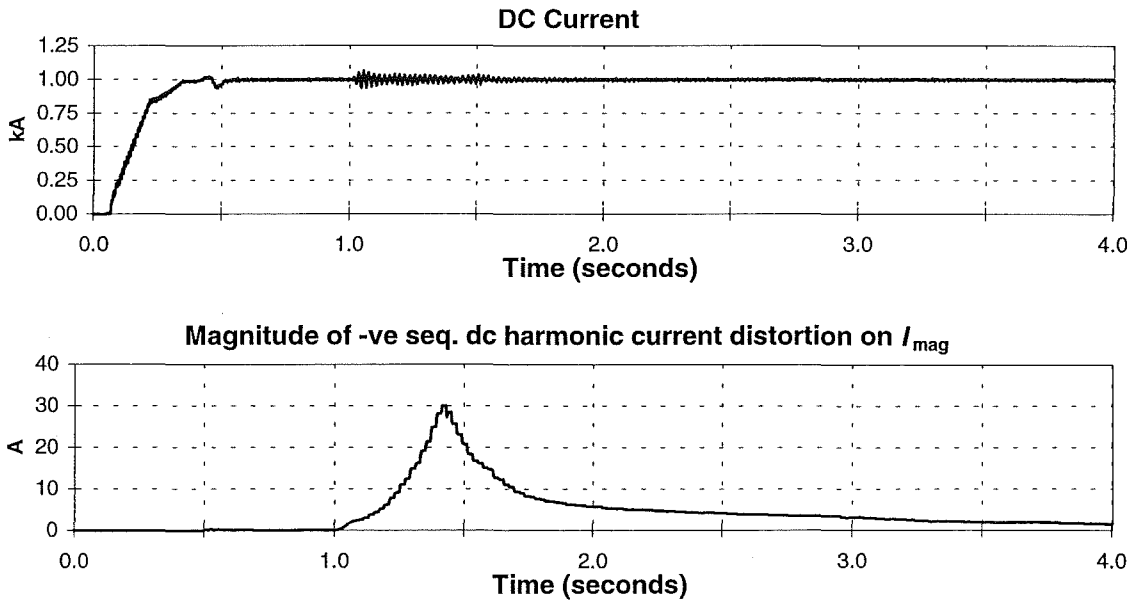


Figure 5-5: Simulation results of test system with additional ac harmonic filter

A similar stabilising effect can be achieved by altering the convertor dc side impedance. Figure 5-6 shows the *SSF* of the test system for different values of an additional dc smoothing reactor at the rectifier end. The system will become stable with an additional smoothing reactor of more than 0.3H inductance.

For an additional inductance of 0.5H, the system *SSF* has a positive value of 0.566. Again, the stability of the system is confirmed by simulation as shown in Figure 5-7. The increase in dc side inductance shifts the resonance frequency from 57Hz to 47Hz, forcing the dc side impedance at the fundamental frequency to become inductive, which is one of the conditions for stability.

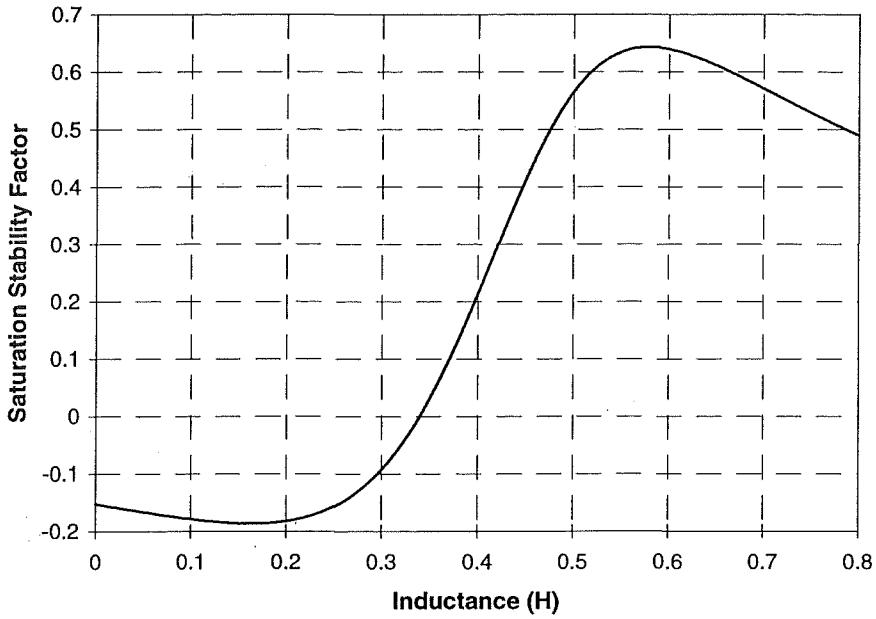


Figure 5-6: *SSF* versus inductance of additional dc smoothing reactor

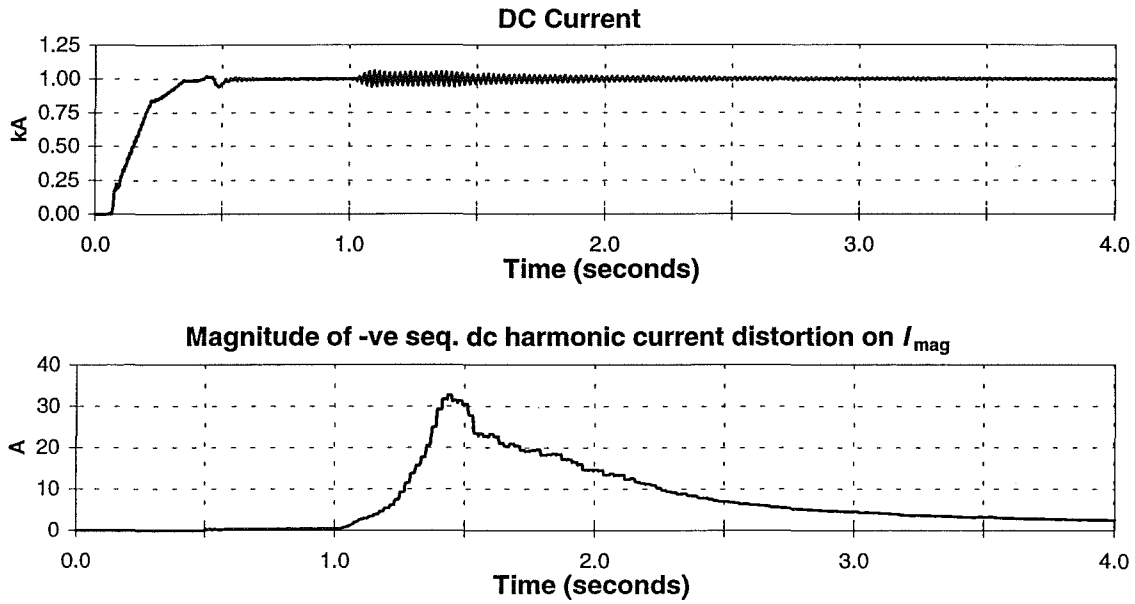


Figure 5-7: Simulation results of test system with higher inductance dc reactor

5.3.2 *Changing the convertor operating conditions*

In addition to the characteristics of the system impedances, the susceptibility to the core saturation instability also depends on the steady state operating conditions of the HVDC system. In the previous chapter, the steady state operating conditions are characterised by the convertor firing angle and length of the commutation process. Figure 5-8 shows the *SSF* of the test system under different convertor firing angles and illustrates that a higher firing angle will destabilise the system. Therefore, the instability problem can be solved by lowering the convertor firing angle under normal operation. Reducing the convertor firing angle also lengthens the commutation process, thereby raising the apparent damping in the system. At an angle of 10°, the commutation angle is increased to 25.72° and the *SSF* becomes positive at 0.087 indicating stability. This prediction is validated by the simulation results shown in Figure 5-9.

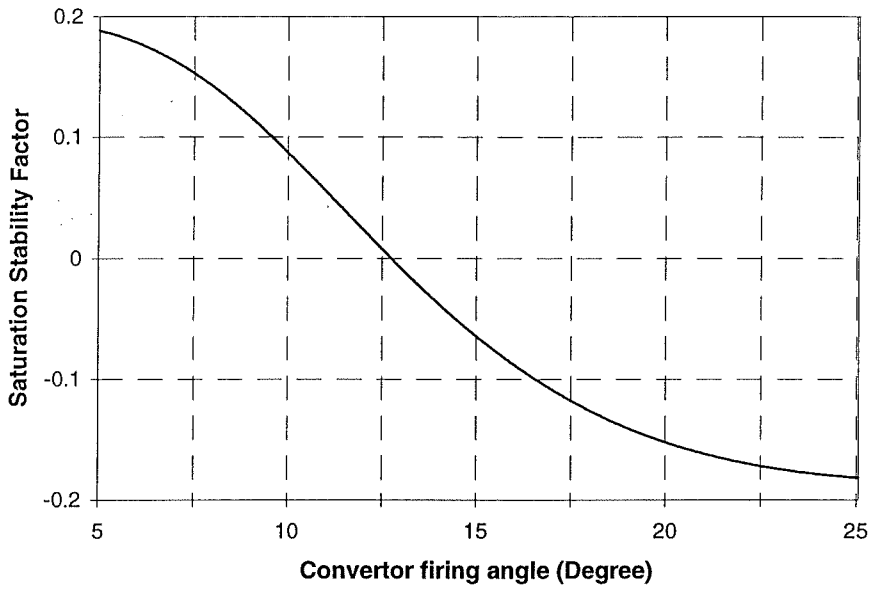


Figure 5-8: *SSF* versus convertor firing angle

Although this example illustrates the effect of convertor firing angle variations, other steady state operating parameters such as the dc current can also be altered to improve the system stability, and the *SSF* approach can be equally used to decide the most appropriate setting. In certain cases, a combination of several changes to the steady state operating parameters may be required in order to counter the instability.

5.3.3 *Alteration to the convertor controller parameters*

It has already been described that the onset of the instability is likely to include some contribution from the convertor controller. In a similar way, it is possible to strengthen the system through proper tuning of the convertor controller parameters. The *SSF* approach with its ability to show the relative stability of different controllers provides a convenient way of determining the configuration of the convertor controller. Figure 5-10 shows the *SSF* of the test system calculated over a wide range of responses of the constant current controller used at

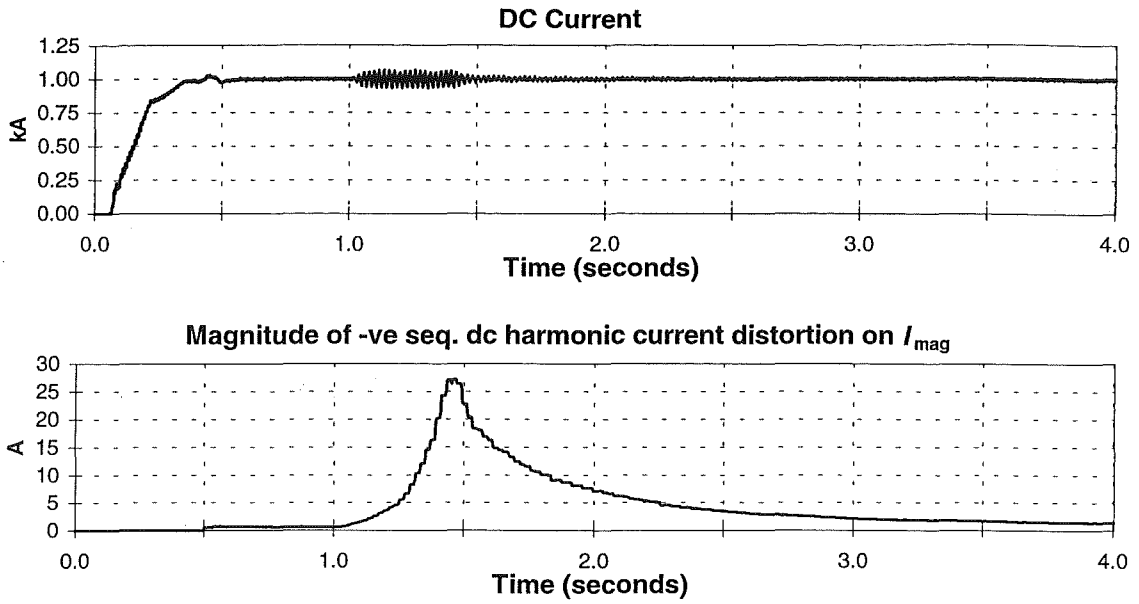


Figure 5-9: Simulation result of test system with low convertor firing angle of 10°

the rectifier. It shows that the system is unstable when the convertor controller has a rather high gain, above 1.2 radian/per unit dc current and with some phase lag. The figure also shows that the unstable *SSF* can be raised to become positive by lowering the gain magnitude and by raising the phase lag.

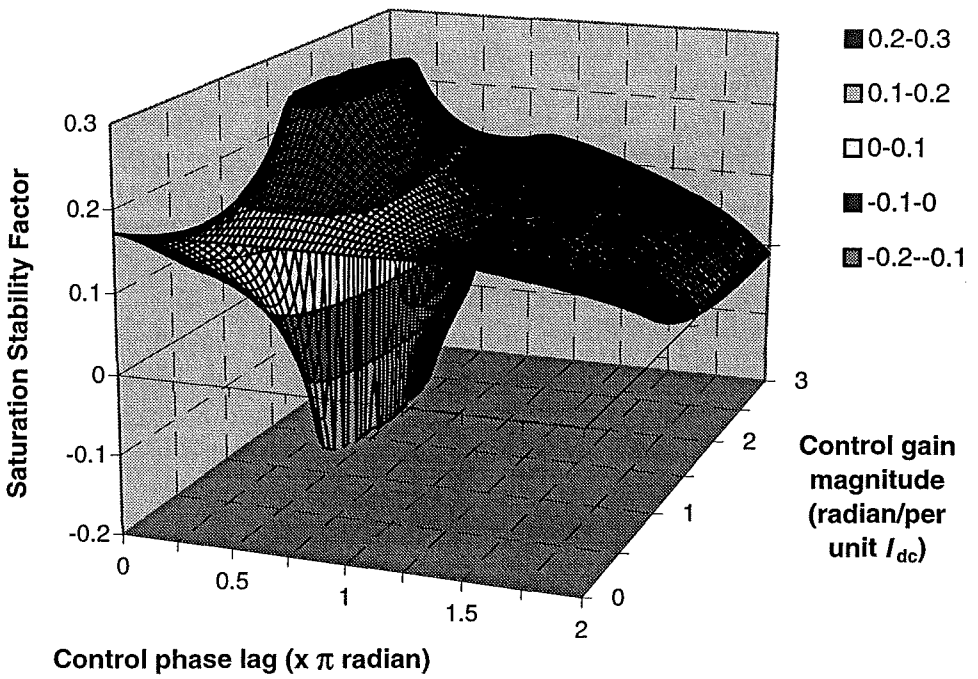


Figure 5-10: *SSF* versus convertor controller frequency response

The convertor controller used in the unstable base case shown in Figure 5-3 was deliberately chosen to fall within the negative *SSF* region, with gain magnitude of 1.5 radian/per unit dc

current and phase lag of 0.25π. If the controller response is altered to 1.0 radian/per unit dc current magnitude and 0.40π phase lag, the *SSF* changes from -0.152 to positive at 0.232. It would be expected that the test system will become stable with the new controller configuration. The simulation of this test case has verified the prediction, as shown in Figure 5-11. The selection of this convertor controller configuration is oriented solely at the prevention of the core saturation instability. In practice, other requirements or constraints on the system have to be taken into account alongside the prevention of this instability to arrive at an appropriate controller configuration for the particular scheme.

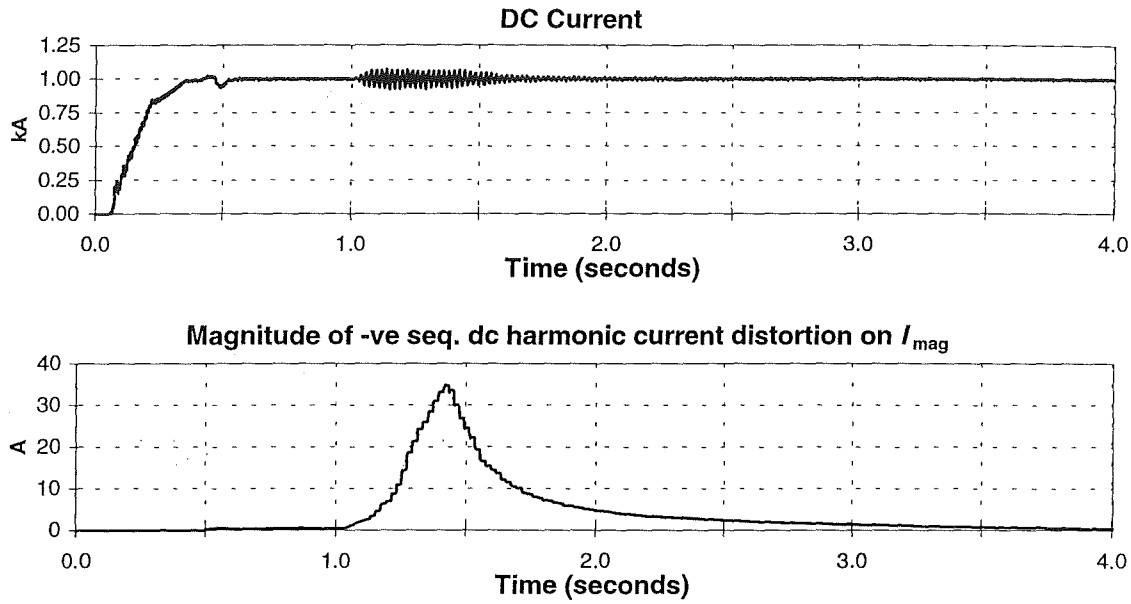


Figure 5-11: Simulation result of test system with modified convertor controller

5.3.4 Auxiliary convertor controller

The concept of incorporating an additional control loop around the main convertor controller for solving the instability is not new and has been used successfully in several installations, [Ainsworth, 1977] and [Hammad, 1992]. This method involves monitoring of the distortion at the relevant frequencies and introducing a modulation signal into the main control loop according to the extent of the distortions. In the Kingsnorth scheme [Ainsworth, 1977], the second harmonic in the transformer magnetising current is measured and used to estimate the level of saturation on the transformer. The three measured signals per bridge are combined to form a single modulating signal which augments the common control signal. An auxiliary dc control scheme has been implemented in the Chateauguay system to damp the fundamental frequency oscillations in the dc current. The distortion is measured and the signal is passed through a proportional and integral controller before being used to adjust the rectifier firing angle.

One major benefit of using an auxiliary controller is that the HVDC scheme can be operated as usual under normal conditions. The auxiliary controller is normally tuned to function over a limited range of frequency, and can be active only when the onset of the instability is detected. This method is particularly advantageous when the requirements or constraints on the system prevent the use of other passive control techniques.

The limited range of operational frequency postulates that the auxiliary controller may be implemented using tuned control filters. This method was used in [Bodger *et al.*, 1990] to damp the oscillations at several frequencies in a simulated bipolar dc link. The output of a fast response dc current transducer was fed through several filters and a gain, and was added to the firing angle order of the rectifier. A number of filter configurations were found to be effective in reducing the harmonic distortion but none more so than a high pass filter tuned to a frequency below the fundamental frequency. This method is tested in this section for countering the core saturation instability and the *SSF* approach is used to derive the filter coefficients.

Figure 5-12 shows the addition of the auxiliary controller to the control loop of the PI controller block in the rectifier constant current controller. Under normal operating conditions, the main PI controller is used to maintain the required dc current on the link. With the presence of core saturation instability, the measured dc current will contain harmonic distortion including that at the fundamental frequency. The distortion will pass through both the main PI controller and the high pass filter auxiliary controller. The outputs from the controllers are added to form a single firing angle order. The auxiliary controller is designed in such a way that the resultant firing angle order causes sufficient damping to be generated in the system to prevent the onset of the instability. This can be achieved by tuning the parameters of the high pass filter to maximise the *SSF* of the system.

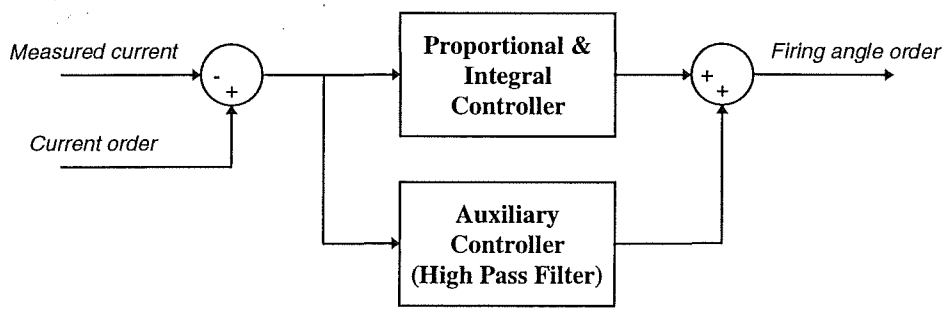


Figure 5-12: Simplified diagram of auxiliary convertor controller connection

The transfer function of a second order high pass filter can be expressed as equation 5.1 with three coefficients, the filter gain (G), the damping ratio (ζ) and the cut-off frequency (ω_0). In the following section, the *SSF* approach is used to arrive at the most appropriate settings for these coefficients such that the system *SSF* is maximised.

$$H = G \times \left(\frac{\left(\frac{j\omega}{\omega_0}\right)^2}{1 + 2\zeta\frac{j\omega}{\omega_0} + \left(\frac{j\omega}{\omega_0}\right)^2} \right) \qquad \textbf{(5.1)}$$

The filter cut-off frequency is first set at the fundamental frequency of 50Hz and the *SSF* of the test system is calculated for different values of filter gains and damping ratio. These two *SSF* curves are shown in Figure 5-13 and Figure 5-14. When the cut-off frequency is tuned to 50Hz, the system stability improves with the filter gain but remains relatively unchanged for different values of damping ratio. From these figures, the filter gain is selected to be 3.0 radian/per unit dc current while the filter damping ratio is set to 0.5. With these settings, the

cut-off frequency of the filter is then determined from the evaluation of the *SSF* for a range of frequencies. Figure 5-15 shows the *SSF* of the test system improves with the increase in frequency and peaks at around 90Hz. 80Hz is chosen as the cut-off frequency and the relationships between the *SSF* and the filter's gain and damping ratio are reevaluated. This procedure can be reiterated to arrive at appropriate settings, but for the purpose of this illustration, the filter's coefficients are set at this stage to a gain of 3.0 radian/per unit dc current, 0.5 damping ratio and cut-off frequency of 80Hz.

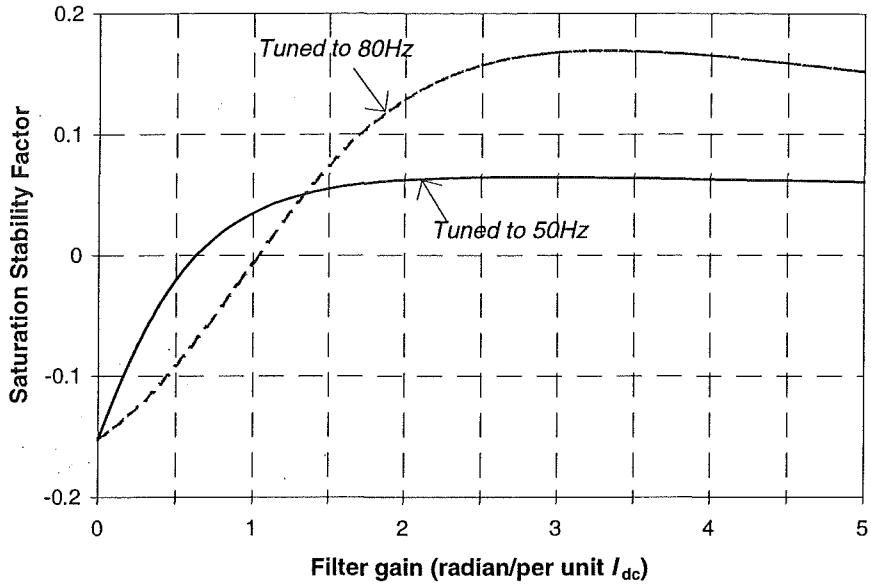


Figure 5-13: *SSF* versus the gain of high pass control filter

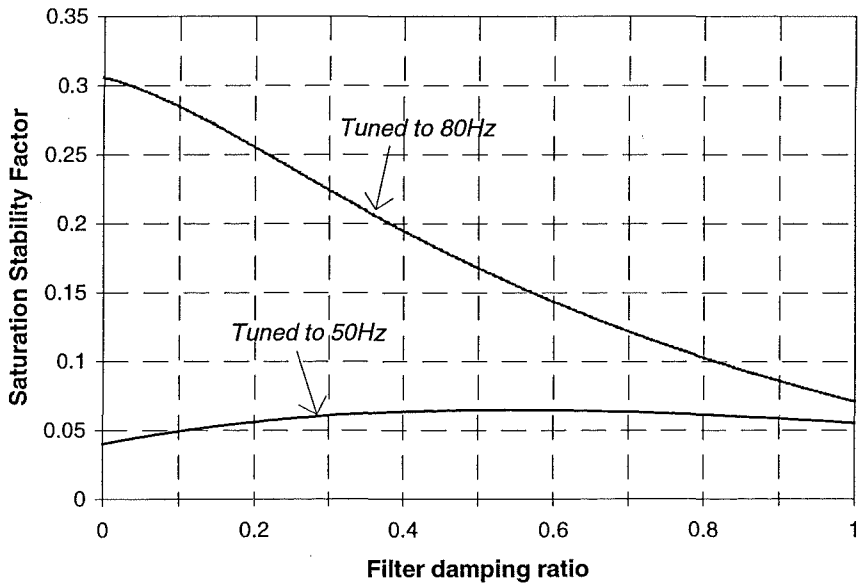


Figure 5-14: *SSF* versus the damping ratio of high pass control filter

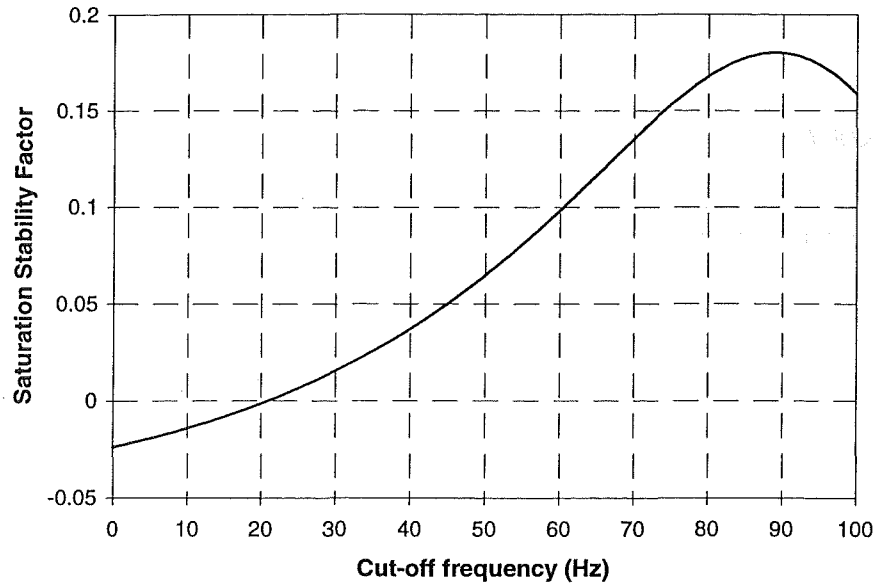


Figure 5-15: *SSF* versus the cut-off frequency of high pass control filter

With the high pass filter incorporated as an auxiliary convertor controller, the system *SSF* is raised to 0.168. The simulation results of this scheme are shown in Figure 5-16 confirming that the addition of the high pass filter as an auxiliary convertor controller has generated extra damping at the relevant frequencies and thus assisted in preventing the development of the instability.

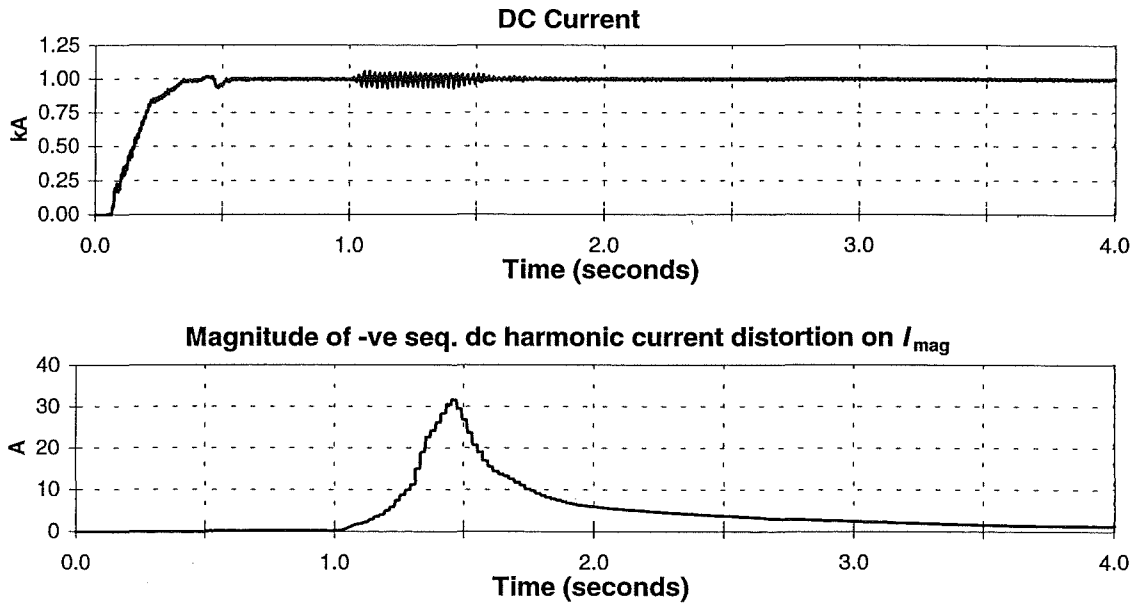


Figure 5-16: Simulation results of test system with high pass filter auxiliary controller

A similar approach has been attempted with a second order band pass filter but was unsuccessful due to another resonance problem in the test system. The CIGRE HVDC benchmark model contains a composite resonance around 70Hz [Wood *et al.*, 1995b], which

also exists in the modified test system. The range of band pass filter gain suitable for preventing core saturation instability is found to be too high around 70Hz and tends to excite the composite resonance.

5.4 Conclusion

The illustrations in this chapter have highlighted the strength of the *SSF* approach in the design of control measures to counter convertor transformer core saturation instability. Its ability to distinguish between very effective and less effective solutions has provided a convenient way for comparing different control configurations. The overview of the problem not only reveals the unstable operating conditions that are to be avoided, but also has pinpointed appropriate measures to be used for its solution.

The control methods described in this chapter are not new but the availability of the *SSF* approach has been shown to greatly simplify the design process. The direct indication of system stability by the *SSF* has eliminated the heuristic process and trial experiments that are reluctantly employed in most analyses. The most effective control measures can be easily reached by comparing the *SSF* of different schemes. However, it is important to bear in mind that the *SSF* only shows the system core saturation stability. In most HVDC schemes, there are several instabilities including those involve harmonic interaction around the convertor to be prevented and controlled. Therefore, it is necessary to verify that any control measures derived from the *SSF* approach to counter the core saturation instability do not enhance other types of instability.

Chapter 6

Flexible Real Time Data Acquisition System

6.1 Introduction

Practical measurement usually plays an essential role in power system analysis. Sound data acquisition systems are required not only for field measurements but also in real time simulation studies. The simulation of harmonic instability with long time constants, such as convertor transformer core saturation instability, requires a compatible data acquisition system in order to carry out comprehensive analysis in real time. Such analysis places a considerable demand on the capability provided by a data acquisition system. The ability to acquire, process, analyse and store data on a continuous basis in real time without any break in the incoming data has to be carefully designed into the system. Despite the vast advancement in computer hardware and software, the majority of these requirements have not yet been achieved by existing commercial data acquisition systems.

Existing data acquisition systems are designed either in too general system configurations or as dedicated systems for predefined and limited applications. Consequently, it is often difficult to and sometimes impossible to accomplish all the tasks needed when making real time measurements. In some cases, several systems have to be assembled in order to undertake all the measurements needed for specific analyses. Any deviation from the instrument's predefined usage generally requires much additional effort and capital investment. Moreover, the measured result can usually be manipulated only within the data acquisition system itself and is often incompatible with other data analysis and presentation packages. In summary, users are forced to manipulate their measurements in several ways to match the various requirements of different processing packages in order to complete their assignments. This means that the analysis of power system is largely constrained by the capability of existing data acquisition systems.

There is also a need for a flexible research tool with the capacity to test new measuring techniques. In particular, the detection of core saturation instability development requires knowledge of specific harmonic distortions in sequence format which cannot be easily accomplished with conventional data acquisition systems. At the moment, to perform such tasks researchers have to construct their own prototype systems complete with all of the rudimentary hardware and software such as hard disks and user interfaces. With current advances in computer hardware and software, it should be possible to construct a flexible system to allow new customised hardware and software to be incorporated into the system with minimal labour. This will reduce the time and cost involved in developing new ideas and enable the researchers to concentrate on deriving and perfecting the new techniques, instead of wasting their effort on assembling basic components or programming rudimentary data storage routines and fancy user interfaces.

The various requirements of such a flexible data acquisition system are outlined in the next section and this is followed by a brief introduction to a data acquisition system called CHART which addresses most of these issues.

6.2 Requirements

Apart from the requirements expected from a basic data acquisition system, there are several unique qualities needed to be addressed in a flexible system. These qualities distinguish a flexible research tool from other standard data acquisition systems. Only with these features, the analysis of power system would not be compromised by the lack of certain capability in the data acquisition system.

Firstly, the system must provide flexibility in the number of data channels, capable of being extended according to the needs of the user. Secondly, it should be able to acquire and process data continuously (i.e. non snap shot) in real time so as to prevent the possible lost of events which happen in between the snap shots. Furthermore, it must be possible to synchronise the continuous acquisition of data across the multiple channels. In certain circumstances, data from different channels are to be brought together for further computation in real time, indicating the need for processing data in successive stages. Finally, there is a need for precision time-tagging so that data acquired at different parts of a power system can be matched up in time. These requirements call for a hierarchical layer of processors to implement such a concurrent data processing. It also requires a centralised and accurate timing source to synchronise all of the data acquisition process and to time-tag the acquired data. Advancement in the GPS (Global Positioning System) technology has greatly enhanced this opportunity but surprisingly none of the existing systems has taken full advantage of this innovation.

Although most of the existing systems allow users to "set up" the calculation procedure, they are usually unable to implement users' customised computation algorithms. Such an undertaking with existing systems usually requires costly modifications or extensions to the systems. Furthermore, the lack of familiarity with the system delays the development process and costs doubts about the effectiveness of the final system. Within the research arena, new algorithms surface regularly and need to be tested or experimented with on an on-going basis. Therefore, a flexible research tool must allow such activities to be carried out with minimal effort at the implementation phase. This allows the emphasis to be placed on developing the algorithms rather than re/designing new data acquisition hardware for every application. Therefore, the architecture of a flexible system must have provision for new algorithms to be readily added to the system. The additional ability to dynamically alter the routine to be used in the system would greatly assist in moulding any new idea into practical reality.

Any basic data acquisition system must allow the acquired data to be displayed in real time and to be stored for further processing or analysis at a latter date. However, most instruments have only standard displays which may not be easily reconfigured to become compatible with customised data formats resulting from customised processing algorithms and applications. Moreover, the systems are usually inflexible, unable to implement new types of display and unable to accept other data formats besides the standard built-in formats. These deficiencies must be addressed in a flexible data acquisition system. Customised display must be able to be designed and incorporated into the system with ease alongside the new algorithms or applications. A new processing algorithm not only produces new data formats but also requires new set-up procedure and new set-up parameters. These features would have to be included in the design of a flexible system.

Although most systems are able to store acquired data, constraints such as the system throughputs and the amount of available storage space tend to limit the storing frequency, the amount of data that can be stored and consequently the time duration over which any monitoring exercise may be carried out. One way of countering this problem is to carry out the data processing and analysis in real time, and store only those details required for further analysis or recording purposes. This further emphasises the importance of the ability to incorporate new on-line computation and analysis algorithm. Furthermore, the storage system must be able to handle the varying nature of data formats expected from different algorithms. The resolution and accuracy of the acquired data must be preserved in the storage process.

The ability to store data in variant formats would be disadvantaged if the stored data cannot be easily retrieved for analysis. At the moment, the data stored in most instruments are not generally compatible with other post-processing tools although there is a trend towards wider compatibility. Instruments such as Fluke NetDAQ (Network Data Acquisition Tools) allow the acquired data to be imported into general purpose analysis software packages such as Microsoft Excel spread sheet program. However, there is still room to streamline the process of transferring the data into these packages. It remains an extremely elaborate and time consuming process, particularly when the measurement has been undertaken over long periods of time, amounting to megabytes of data. The use of indices in commercial databases to aid locating information quickly has so far not been utilised in power system measuring instruments. This is rather surprising considering the vast quantity of data expected in the majority of power system measurements. The limitations of low throughput/bandwidth or insufficient storage space in existing data acquisition systems tend to keep the data storage volume relatively small which perhaps negated the need for such an efficient mechanism. Therefore, the flexible system should provide easy and quick access to the stored data either through the user's customised software program or through commercially available general purpose analysis and reporting packages.

One of the major requirements of any data acquisition system is the potential for future expansions such as replacing old processors with new faster and more powerful versions or introducing additional components to perform certain application specific functions. Therefore, a flexible data acquisition system should allow new series of hardware components to be added into the system while still using the basic core functions of the system to set-up the new components and to collect data for display. Normally, a general purpose system possesses a fairly wide bandwidth which is sufficient for most applications. However, specialised studies such as capturing of transient waveforms require special high speed data capture front ends equipped with fast reacting signal conditioning circuitry. Therefore, the structure of the acquisition system should allow such specialised extensions to be included as part of the system.

Besides the above specific requirements, the system must also adhere to other common prerequisites such as conforming to certain rules and regulations, providing a graphical user friendly interface and compliance with various safety standards. In summary, a flexible data acquisition system has to fulfill all the basic requirements of any data acquisition system and perform all the house-keeping chores while allowing the users to incorporate customised hardware and software components with minimal effort.

6.3 CHART system

The measurement of harmonics is currently achieved by processing snap shots of captured information. This method is sufficient provided the harmonics in the system remain constant

long enough for it to be captured by successive snap shots. However, this method becomes inadequate if the harmonics are constantly varying such as in systems with arc furnaces. In such cases, the harmonics have to be analysed continuously in real time in order to appreciate the extent of the problem.

In an effort to overcome the above problem, the development of a data acquisition system called CHART (Continuous Harmonic Analysis in Real Time) was initiated in the mid-80's and since then has gone through several cycles of development. Its major strength lies with its ability to continuously monitor every single data sample in real time which ensures that no event is lost. Furthermore, the use of accurate GPS satellite system allows accurate time-stamping of the captured data samples and hence for the first time enable true time linkage to be established for data monitored at different points of the power system network.

CHART has been successfully used in several field measurements with very encouraging results and it was the experience gained from these exercises that indicated the under utilisation of the capabilities of the system. Furthermore, the distributed nature of the system initially designed to reduce interference to the measuring signals has lend itself to easy extensions for other applications. Therefore, with the opportunity to fine-tune the architecture of the system in the late 1993, the structure of the system, particularly the software architecture, was redesigned to fulfill the requirements of a fully flexible data acquisition system. The aim was to extend the use of the CHART system to other research activities within the power system group at the University of Canterbury, while maintaining the harmonic monitoring as one of its prime functions. The real time analysis of the convertor transformer core saturation instability was one of the prime motivations in undertaking such a development.

A brief historical review of the CHART system is presented in Chapter 7, and this is followed by a description of the hardware components making up the latest system, CHART III. The software architecture which exploits the distributed parallel processing structure of the system, and which makes it possible for the system to be applied to other purposes is described in Chapter 8. Lastly, the two different field applications of the CHART III system which have demonstrated its versatility are presented in Chapter 9.

Chapter 7

Description of CHART III System

7.1 Introduction

The CHART system started with a centralised processing system, CHART I, which has been described in several publications [Miller *et al.,* 1989], [Lake *et al.,* 1990] and [Miller *et al.,* 1990]. Although it was successfully used in several field measurements [Miller, 1990a], it was soon realised that it possesses little room for expansion. Moreover, the close-knit nature of the functions performed by each of the processors rendered the system inflexible and difficult to be adapted for other purposes. These constraints and the availability of a growing number of more powerful and yet lower cost processors compelled the restructuring of the system in the early 90's.

The development of CHART II saw the shift from a centralised processing system to a modular system with processing power distributed throughout the system. The distributed architecture of CHART II [Miller *et al.,* 1992] has increased the capabilities of the system substantially and introduced its flexibility. One of the factors contributing to the success of CHART II was the advancement in the DSP (Digital Signal Processor) technology, enabling the amalgamation of the various functions performed by several processors in CHART I into a single DSP in CHART II. Several field measurements were made with the CHART II system on the upgraded New Zealand HVDC link [Miller *et al.,* 1994]. However, the software architecture was designed solely for measuring harmonics, even though the structure of the hardware is capable of performing other functions.

In 1993, as a result of one of the key processing boards used in CHART II being discontinued by the manufacturer, redevelopment of the CHART system became necessary. At the same time, the secure of sales of several systems forced the development of the CHART III system to be completed within a short time span in 1994. The hardware structure of CHART III is similar to that of CHART II, but it was constructed with more industrial standard components. A number of other hardware design features were also upgraded. In line with the redevelopment, the architecture of the software was revised and redesigned to expand the capability of the CHART system beyond harmonic measurement. The main motivation behind this decision was the need to provide a flexible tool for use in the power system research activities at the University of Canterbury.

A review of the CHART I and CHART II systems is presented in the next section, followed by an overview of the architecture of the new CHART III system. The major components making up the CHART III system are further described in this chapter, while the software design is detailed in Chapter 8.

7.2 Review of CHART I and CHART II

The CHART I system is based on an Intel Multibus II [Multibus II, 1987] multi-processor system, with each processor performing a specific task as shown in Figure 7-1. It makes use of 286/386 processors which were state of art processors at that time. The use of DSP was considered but was later rejected due to the prohibitively high cost.

A 6-channel data acquisition system was specifically designed for the purpose of acquiring six analog signals simultaneously from external transducers, and converting them into digital samples. The digitised data is transmitted through the SBX (System Bus eXtension) bus to the Multibus II system for processing. The Multibus II system acts as the central processing system, performing all the numerical computations. The collected samples were averaged over several cycles of the system fundamental frequency in the Acquisition Processor. This averaging process reduces several cycles of data into a single cycle and hence reduces the amount of computation required to process the data. The averaged samples are then Fourier-transformed to extract the frequency information using a FFT algorithm in the FFT Processor. The calculated harmonics are transferred to the Compaction and Storage Processor which selectively stores the relevant harmonics into a hard disk. It also dispatches the harmonics through a GPIB bus (General Purpose Interface Bus) to a PC/AT for display. Within the Multibus II system, the processor boards communicate with each other using a message passing protocol via the iPSB bus (Parallel System Bus).

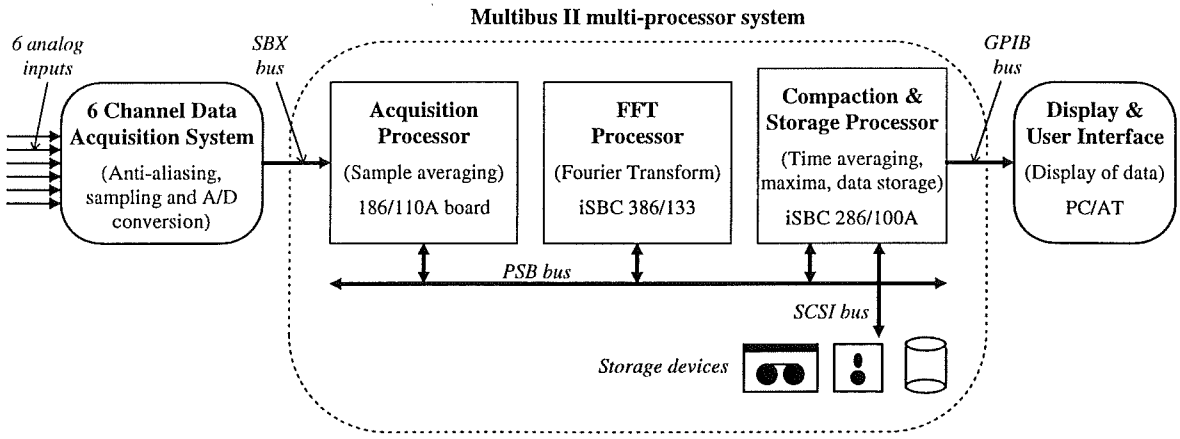


Figure 7-1: CHART I system overview

The structure of CHART I was oriented to measure harmonics in power systems. Due to the level of technology at that time, the data processing had to be spread out over several processors. Although it possesses a parallel processor structure, it was used in a serial manner with the captured data being transferred from the Acquisition Processor to the FFT Processor, and finally to the Compaction and Storage Processor. Excessive use of the iPSB bus for data transfer has left little room for the system to expand beyond six channels. Nonetheless, it was the first instrument capable of capturing and processing multiple channels of samples simultaneously and continuously in real time.

The CHART II system was a substantial improvement on its predecessor although a similar bus system was used. Figure 7-2 shows the architecture of CHART II, broadly made up of three parts, the RDCM (Remote Data Conversion Module), the PPU (Parallel Processing Unit) and the CADU (Control And Display Unit). The RDCM was designed as a single-channel portable analog to digital conversion unit, fully equipped with the front end signal

conditioning circuitry. It converts the analog current transformer or voltage transformer outputs to 16 bit digital signals, and transmit them to the PPU via a fibre optic link. This separation of the RDCM from the main processing unit of PPU facilitates the tailoring of the analog to digital conversion circuitry to particular application requirements in a functional and cost effective way. Furthermore, the use of digital communication through the fibre optic link has greatly increased the dynamic range of the system.

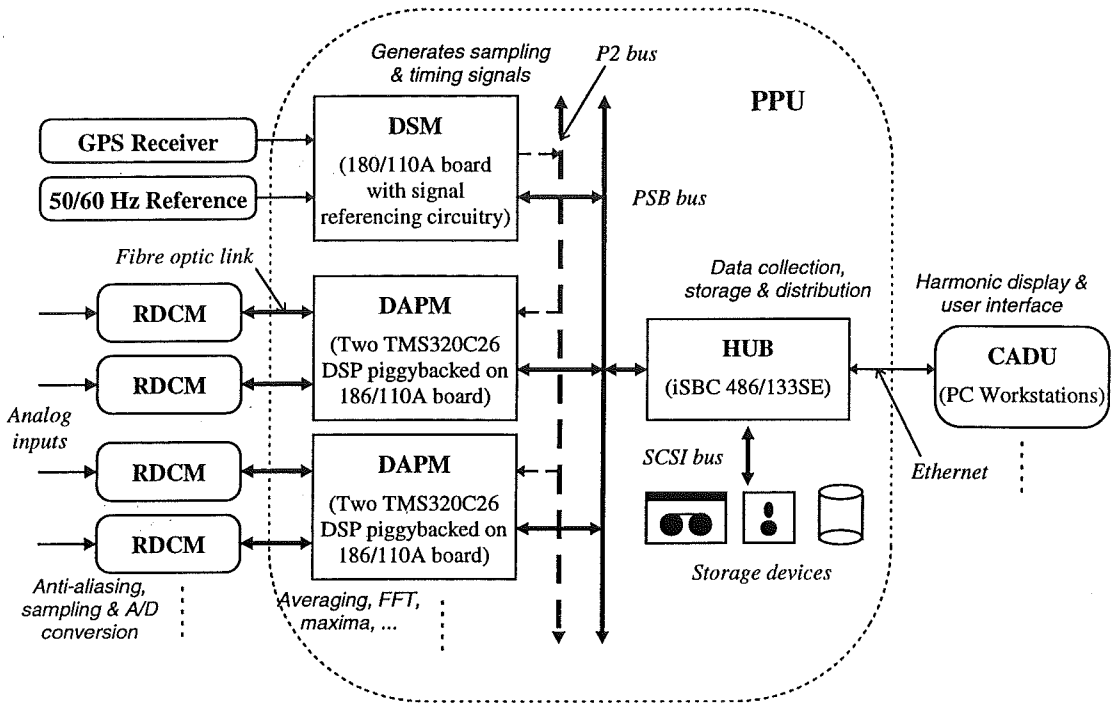


Figure 7-2: CHART II system overview

The PPU is based on the Intel Multibus II architecture and there are four different kinds of processor boards in the unit. The DAPM (Data Acquisition and Processing Module) is made up of two TMS320C26 DSP's, both connected through FIFO (First In First Out) to a 80186 processor. Each DSP receives digital samples from an RDCM and carries out the FIR (Finite Impulse Response) filtering with decimation to reduce the number of samples per fundamental cycle, and the FFT to derive the harmonic components. The computed harmonics are then passed to the 80186 which monitors the harmonic averages, maximums, etc. The DAPM also receives precise sampling pulses from the P2 bus and redirects these pulses to the RDCM. These pulses are generated by the DSM (Digital Services Module) with reference to the mains fundamental frequency. The DSM also generates accurate time-stamping signals based on the precision date and time information received from the GPS receiver. This centralised control of the sampling pulses enables synchronisation of the sampling process across all RDCM's. The accurate timing signals are transmitted to the HUB through the iPSB bus. The HUB acting as the central collecting and distributing point of the system, receives computed harmonics from the DAPM's. It functions as a data client requesting harmonic data from the DAPM's and timing information from the DSM. Each of the collected harmonics are time-tagged with the time received from the DSM. The HUB is also programmed to store the calculated harmonics in a hard disk at regular interval, and to distribute the data to the CADU for display.

The CADU is based on a 386/486 PC capable of running Microsoft Windows Version 3.1. Its primary function is to display the calculated harmonics and other relevant data in real time. It also provides user interfaces for controlling the operation of the entire system. It interfaces with the HUB via the Ethernet network.

The modular architecture of the CHART II system has the potential of being tailored for other applications such as transient analysis. However, the structure of the software in the various processors is again closely integrated, making it difficult to adapt to other applications. Moreover, the supported data formats are limited to those related to the analysis of steady state harmonics in the power system. Nevertheless, it was successfully used in several harmonic field measurements which have demonstrated its computation capability. However, the software needed to be revised in order to allow the system to be used for other purposes.

7.3 CHART III system overview

The CHART III system has an identical structure to its predecessor but with several improvements on the front end modules and the data processing modules. The most significant change is the adoption of the MIX (Modular Interface eXtension) bus system [MIX, 94] to interface with the DSM and DAPM boards. Figure 7-3 shows the structure of the CHART III system comprising of multiple front end interfaces to the transducers of a series of RDCM (Remote Data Conversion Module), a parallel data processing system of a PPU (Parallel Processing Unit) and a network of workstations referred as the CADU (Control and Display Unit).

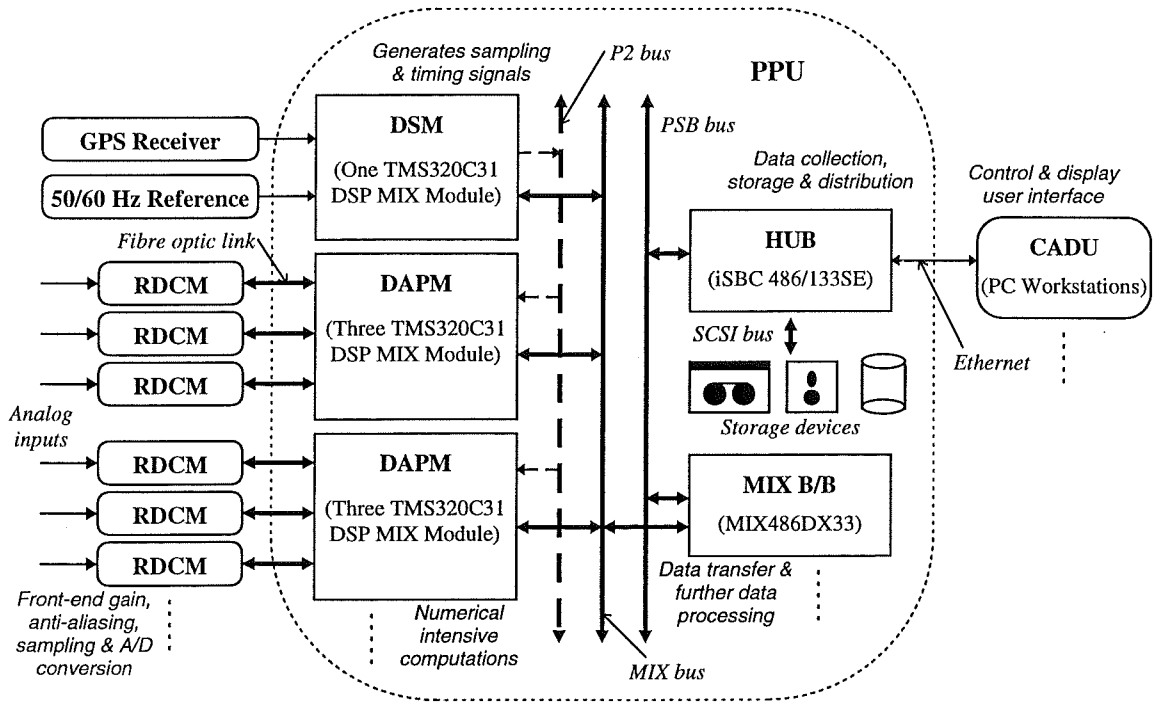


Figure 7-3: CHART III system overview

The RDCM has similar functionality to its predecessor, but is refined with several attractive features. Each analog signal originating from a transducer is converted into digital signal representation by the RDCM and transmitted to the PPU by fibre optic cable. The RDCM is designed to be situated close to the transducers, isolating the CHART computer systems and

users from potential hazardous voltages under fault conditions in the switch yard. Furthermore, the use of fibre optic links between the conversion modules of RDCM and the processing system of PPU eliminates the problem of ground loops in the instrumentation system. It also reduces the electromagnetic and electrostatic noise interference and pick-up which can be enormous in an electrical switch yard environment. The quality of the fibre optic link is significantly improved with the use of TAXI [TAXI, 1992] parallel interface and better fibre optic transmitters and receivers.

The digitised signals from all RDCM's are transferred to the PPU for processing, distribution and storage. The PPU is made up of a DSM (Digital Services Module), a series of DAPM's (Data Acquisition and Processing Module), an array of MIX baseboards and a HUB processor. The DSM and DAPM are designed as MIX modules connected to the rest of the system via the MIX bus and through the MIX baseboard. Texas Instrument TMS320C31 floating point DSP [TMS320C31, 1991] are the processors used on these two processing boards. The MIX baseboard and the HUB processor are Intel made general purpose single board computers. They communicate with each other using the Multibus II message passing protocol via the iPSB bus.

The functions of DSM and DAPM in CHART III are similar to those in CHART II. DSM is responsible for generating precision sampling signals used by the RDCM in the sampling process, and accurate time information to time-tag the acquired samples. These signals are dispatched through the P2 bus to the DAPM which redirects the sampling pulses to the RDCM via the fibre optic link, and uses the time information to time-stamp the acquired and processed samples. This design not only enables synchronisation of all the sampling within a single CHART III system, but the use of GPS as the time reference enables true time-linking between the data acquired in different systems. With this feature, the CHART III system stands out among all other instruments as the only one capable of being used simultaneously at different geographical locations with precise synchronisation between the samples acquired in different systems at different locations.

The DAPM carries out the numerically intensive processing of the acquired samples. Typical applications are FIR filtering, FFT and averaging. Each DAPM is capable of receiving samples from three RDCM's simultaneously. The processed data is then transferred to the MIX baseboard through the MIX bus. Apart from acting as the data collecting agent for the DAPM, the MIX baseboard is also responsible for loading the software into the memory of DAPM and DSM. It consists of a Intel 486DX33 CPU which is capable of performing further computation on the data received from the DAPM. Its common applications are the derivation of further information from the combination of data from different DAPM's, and the monitoring of the data for certain programmable events.

The MIX baseboard then transmits the data collected from DAPM together with any newly generated data to the HUB processor. The HUB processor acting as the heart of the entire CHART III system is responsible for collecting, distributing and storing of the data. It is connected to a series of CADU's through the Ethernet network, and with this networking of PPU and CADU, multiple CADU's can be used simultaneously. Apart from sending data to the CADU for display, the HUB processor in return receives control and setup commands from the CADU. Each CADU can be connected to several HUB processors at any one time, enabling the display of data collected at different CHART III systems on a single screen. Using an Internet communication protocol, the CADU and the HUB processor can operate across a WAN (Wide Area Network).

7.4 Remote Data Conversion Module

7.4.1 General description

The RDCM's convert current transducer and voltage transducer outputs to digital signals, and transmit them to the PPU for processing. They are typically located in the switchyard, near the connected current or voltage transducers. Figure 7-4 shows a block diagram of a generic RDCM.

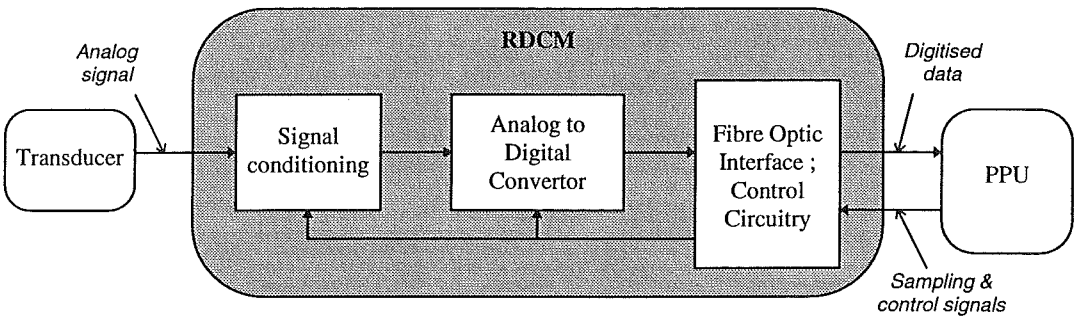


Figure 7-4: Simplified generic RDCM block diagram

The generic functions of the RDCM can be summarised into three functional blocks as shown above. The analog signal received from the transducer is passed through a signal conditioning circuitry. This circuitry typically includes an anti-aliasing filter and some form of amplification, and is designed according to the requirements of the particular RDCM application. The filtered and amplified analog signal is then digitised using a analog to digital convertor. The dynamic range and the resolution of the A/D conversion also depends on the requirements of the RDCM intended application. The analysis of low level high order harmonics requires a high resolution while the capturing of the wave shape of a transient calls for a greater dynamic range. The digitised data is then transferred to the PPU via the fibre optic interface. This interface maintains a full duplex communication with the DAPM in the PPU, receiving sampling and control signals needed for the sample and hold, and the A/D conversion processes, and at the same time returning the digitised data to the PPU. The current version of DAPM described in section 7.5.6 is equipped with a user-configurable fibre optic interface supporting 8, 16, 24 and 32-bit data transmission mode. If the RDCM is designed to be used with this DAPM, the RDCM fibre optic interface has to be compatible with one of the data transfer modes of the DAPM.

Within the modular context of the CHART III architecture, the RDCM is intended to be a stand alone module tailored for a specific application. It is envisaged that it can be powered independently by batteries, providing a degree of freedom in the placement of these modules within a switch yard environment. Alternatively, the RDCM may be designed to be powered from the mains supply which is convenient if the conversion module is to be used in the laboratory. For continuous monitoring without main supply, a solar panel system may be used to supply energy to the RDCM.

The current version of CHART III system comprises a RDCM designated Type A and it is tailored for harmonic analysis. The design of this particular RDCM is described in the next section, followed by a list of possible RDCM's for future expansion.

7.4.2 RDCM Type A for harmonic analysis

The RDCM Type A is tailored to measure harmonics in a power system. It is an improved version of that used in CHART II. It is a single channel system designed to measure either the harmonic voltages or currents in the electrical power system. Figure 7-5 shows the block diagram of this RDCM.

This RDCM Type A has a settable front end gain amplification and attenuation stage that is controlled by the DAPM. Gain settings are received from the DAPM and this changes the amplification on the input signal, thereby optimising the usage of the A/D convertor dynamic range. There are a total of 13 amplification/attenuation gain settings of ÷64, ÷32, ÷16, ÷8, ÷4, ÷2, ×1, ×2, ×4, ×8, ×16, ×32 and ×64. These settings allow the RDCM to monitor analog signals as high as 240 Vrms and as low as 100 mVrms, while still maintaining full usage of the A/D convertor dynamic range. Moreover, this RDCM is equiped with an automatic calibration feature, enabling any shift in the gain of the amplification or attenuation circuitry to be measured and compensated for through software in the DAPM.

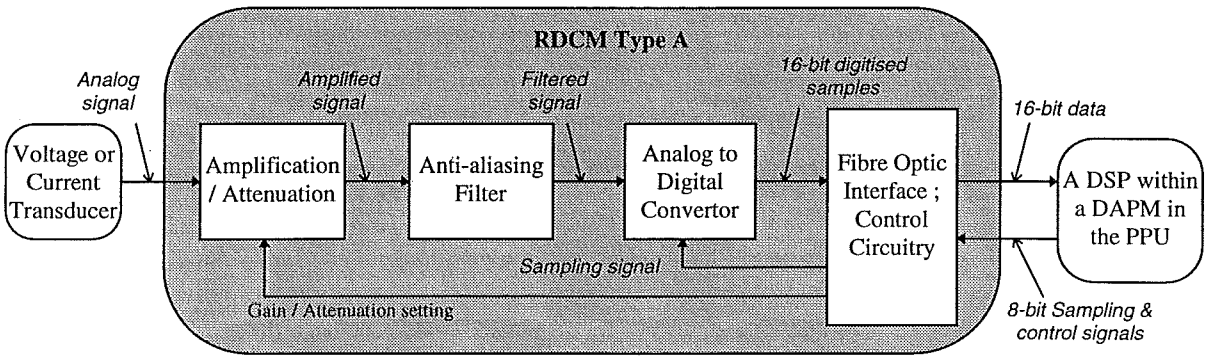


Figure 7-5: RDCM Type A block diagram

The amplified signal is fed through a 5th order Butterworth anti-aliasing filter with cut off frequency of 15 kHz. This cut off frequency is higher than that required for harmonic analysis (which is 3.25 kHz, the 50th harmonic of the 60 Hz + 5Hz of the fundamental), in order to simplify the design of the filter and to reduce its power consumption. This also enables the RDCM to be used to monitor higher frequency components which may be required under future harmonic limit legislation. Furthermore, sampling at high frequency enables different kinds of further anti-aliasing filtering to be implemented using software in the DAPM. This RDCM can be used to sample up to about 70 kHz.

The filtered signal is then converted into 16-bit digital format and transferred to the DAPM via the fibre optic interface. This optical interface is designed to work with the current version of DAPM described in section 7.5.6. The optic receiver operates in 8-bit transfer mode while the transmitter operates in 16-bit mode. This enables the RDCM Type A to receive 8 bit sampling and control signals from the DAPM, while sending 16-bit data back to the DAPM.

The design of the anti-aliasing filter requires that the signal to be sampled at a frequency higher than 30 kHz. It is typically operates at 51.2 kHz for 50 Hz system (or 61.44 kHz for 60 Hz system), resulting in a total of 1024 samples within a fundamental cycle. This mode of operation is tailored for harmonic analysis, facilitating the implementation of FIR (Finite Impulse Response) filtering and FFT (Fast Fourier Transform). Although this RDCM is

designed primarily for monitoring harmonics in the power system, it can also be used for other applications as long as the described design fulfills the application requirements.

7.4.3 Other types of RDCM

Since the modular architecture of the CHART III system allows the design of RDCM to be tailored to specific applications, variants of RDCM are likely to be developed in the future. This section presents a selection of ideas on possible design of RDCM and their probable applications.

Firstly, a multi-channel RDCM has a wide appeal since the ac power system is implemented in three phases. A three-channel RDCM is currently under development at the University of Canterbury and it incorporates a DSP in the design. The amalgamation of three phases into a single channel will be convenient for monitoring three-phase quantities such as sequence components, but the increased processing bandwidth requirement has to be carefully considered. Furthermore, a dual-channel unit with a voltage input and a current input will be useful for monitoring power level and power factor.

Besides multi-channel system, different signal conditioning and filtering circuitry can be implemented for different purposes. For transient analysis, the RDCM must have a high anti-aliasing cut-off frequency with wide dynamic range. It must also be capable of operating at high sampling frequency, typically in the MHz range. A DSP and several memory chips may be required to buffer the captured waveform before sending it to the PPU.

Most RDCM's will be designed for power system analysis, the main purposes of the CHART III system. However, it is not limited to this type of analysis but any activity requiring an able data acquisition system can make use of the CHART III system with specially designed RDCM's. Moreover, the RDCM described here are assumed to be connected to the current version of DAPM. Future development of new types of DAPM's may result in new suites of RDCM's.

7.5 Parallel Processing Unit

7.5.1 General description

The functions of the Parallel Processing Unit (PPU) in the CHART III system can be summarised as follows:

- Receives accurate timing information from the GPS satellite receiver and uses this to generate the sampling and time-stamping signals which are then distributed synchronously to the RDCM's.
- Collects digital samples from the RDCM's and carries out data processing. Data processing includes scaling, compensation, derivation of harmonic information, harmonic parameter calculation, and the ability to implement a wide range of standard as well as customer defined on-line analysis algorithms.
- Provides storage for the acquired data and also distributes the data to the CADU for presentation.

The PPU is based on the Intel Multibus II bus architecture [Multibus II, 1987] comprising of an array of processor boards. The modular structure allows data processing to be distributed over multiple processors and the processing is implemented as close as practicable to the

front end data acquisition stage. This minimises the data bandwidth requirements in the successive stages of processing.

Figure 7-6 shows a typical configuration of PPU but the total number of processor boards in a system depends on the requirements of the application. This flexible configuration allows the system to be tailored to the requirements of specific applications and is described in the next section. There are a total of four different types of processor boards, HUB processor, MIX baseboard, DAPM and DSM, and their individual functions are further illustrated in the following sections. A typical PPU consists of one HUB processor, one DSM, multiple MIX baseboards and multiple DAPM's depending on the user's requirements.

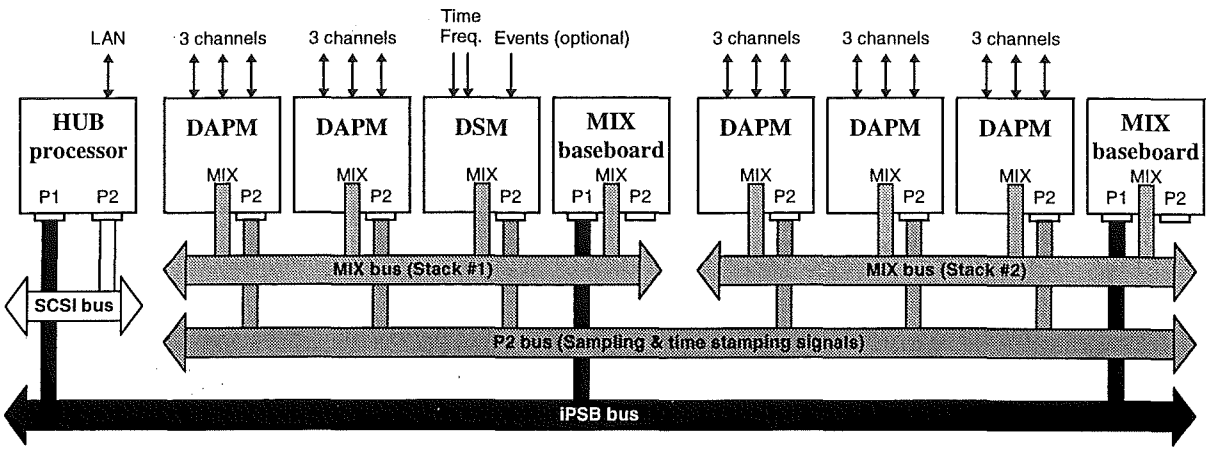


Figure 7-6: A typical PPU configuration

7.5.2 PPU configuration options

The PPU is made up of a Multibus II system with a 12-slot backplane. Each of the processor boards occupies one slot on the backplane. Therefore, the PPU can be configured with any number of boards up to a maximum of 12 boards. This flexible configuration option allows the customers to tailor the system according to their measurement needs and to their budget, while at the same time maintaining sufficient scope for future expansion and upgrade.

Each PPU must have a HUB processor and a DSM with the remaining ten slots being made

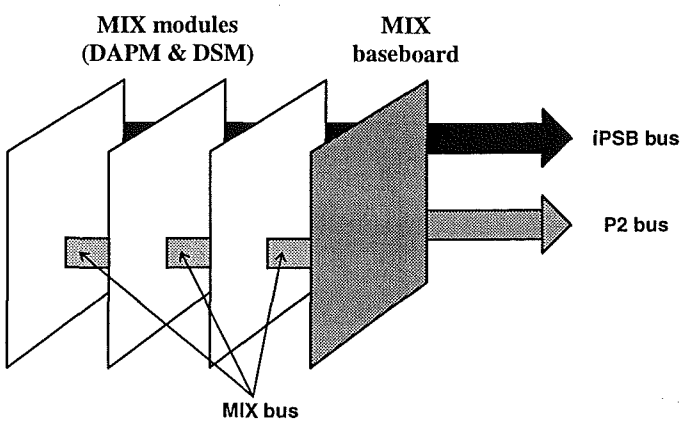


Figure 7-7: Physical layout of a MIX stack

up by the DAPM's and MIX baseboards. The DAPM and DSM are designed as MIX modules which have to be physically attached to the left of the MIX baseboard as shown in Figure 7-7. A maximum of three MIX modules can be attached to a single baseboard, forming a MIX stack.

The need to stack DAPM boards onto the MIX baseboard places a constraint on the utilisation of the remaining ten slots since the HUB processor and the DSM take up one slot each. With such a layout, a minimum configuration is made up of one DAPM as shown in Figure 7-8. There is only one MIX stack in the minimum system allowing a maximum of three digital input channels to be connected to the PPU. On the other hand, the maximum configuration based on the 12-slot backplane has a total of seven DAPM boards and three MIX baseboards as shown in Figure 7-9. There are three MIX stacks with one stack consisting of a DSM and two DAPM's, another stack with three DAPM's and the last stack has two DAPM's. This configuration provides a maximum of twenty-one input channels that can be connected to the PPU.

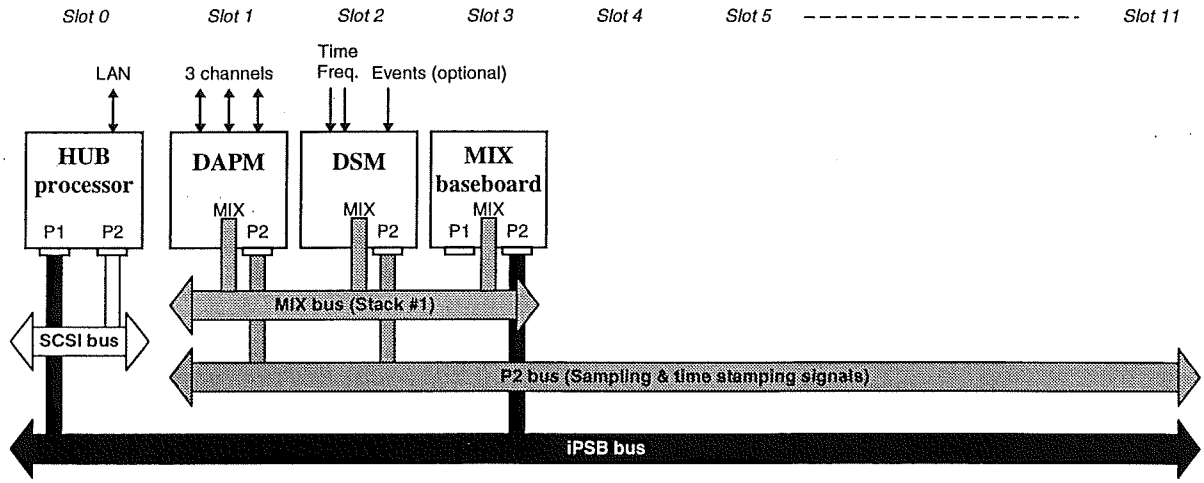


Figure 7-8: Minimum PPU configuration

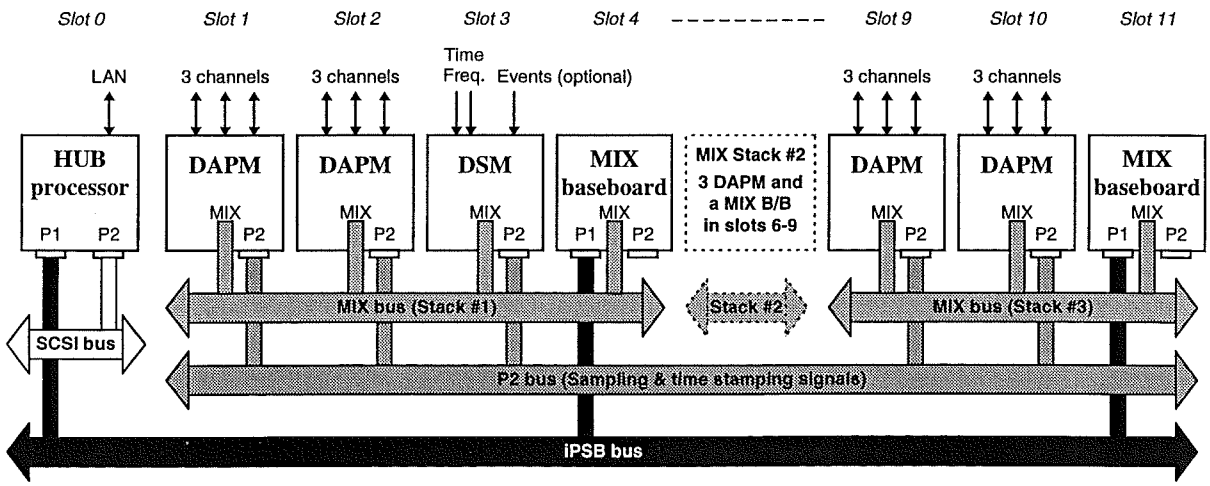


Figure 7-9: Maximum PPU configuration based on 12-slot backplane

The Multibus II system can be expanded up to a maximum of 20 slots. With such a setup, the PPU can be configured with a maximum of 14 DAPMs making a total of 42 digital input channels that can be processed simultaneously within a single chassis.

7.5.3 HUB processor

The HUB processor is an Intel general purpose SBC (Single Board Computer) designed for Multibus II system called iSBC 486/133SE and it is always located at slot 0 of the PPU backplane. This board provides an interface to the Multibus II iPSB backplane which is used to communicate with the MIX baseboard, a SCSI interface to the peripheral storage devices and a network interface to the Ethernet. It uses the Intel iRMX Real Time Multitasking operating system to schedule the initialisation and setting up of the entire PPU, to control the operation of each processor in the system and to coordinate the collection, storage and distribution of the acquired data. It is fully compatible with the Multibus System Architecture and facilitates the initalisation of all of the MIX baseboards within the PPU.

It communicates with the MIX baseboard using the Multibus II message passing mechanism, sending control and setup commands to the MIX baseboard while receiving data and time information that the MIX baseboard collected from DAPM's and DSM. Through the SCSI interface, it stores the relevant data in a hard disk which can be backed up to floppy disks or magnetic tapes. Finally, it uses the network protocol of TCP/IP which is part of the iRMX operating system to communicate with the CADU. Normally, the HUB processor and the CADU's are operated across a LAN (Local Area Network) but with proper software, it is possible to maintain the operation through a WAN (Wide Area Network).

7.5.4 MIX baseboard

The MIX baseboard can be regarded as the manager of the DAPM and DSM. It is an Intel made MIX board with a 486DX33 CPU and is connected to two bus systems, the iPSB backplane which it uses to communicate with the HUB processor and the MIX auxiliary I/O bus to link up with the DAPM's and DSM. It operates with the iRMX operating system similar to the HUB processor. The iRMX operating system provides interface to the message passing mechanism across the iPSB backplane, and transparent access to the hard disk connected to the HUB processor. This latter transparent interface allows the MIX baseboard to retrieve software binaries from the hard disk and load them into the DAPM and DSM. The dual port RAM (DPR) onboard the DAPM and DSM are mapped into the memory space of the MIX baseboard. This mechanism of DPR facilitates the communication between the MIX baseboard and the DAPM and DSM. Despite undertaking the software loading and the transfer of data and time information, the MIX baseboard also possesses sufficient bandwidth to carry out further data processing. User definable algorithms can be initiated as additional iRMX tasks to process data samples received from the DAPM's, while using the same message passing mechanism to dispatch them to the HUB processor.

7.5.5 Digital Services Module

The Digital Services Module (DSM) is designed as MIX I/O module and it has two main functions. Firstly, it provides accurate date and time, and fundamental frequency information to the CHART III system. Secondly, it generates precision sampling and synchronising signals for the data acquisition processes. Besides that, it is also equiped with several event trigger channels including three fibre optic channels, and several digital I/O ports. Figure 7-10

shows the functional block diagram of a DSM. It comprises of a Signal Processor Module and several functional blocks which are the Sample Rate Multiplier (SRM), the Real Time Clock (RTC), the Event Trigger Interface and the Digital I/O Interface.

The SRM is the source of sampling pulses in the CHART III system. It can monitor the power system fundamental frequency and the generation of the sampling pulses can be synchronised to the fundamental frequency. This feature enables coherent sampling which is useful for harmonic analysis. Coherent sampling minimises the spectral leakage from the FFT computation and eliminates the need and added burden of windowing the input samples. The sampling pulses are dispatched through the P2 bus of the Multibus II backplane. The P2 interface consists of a series of latches allowing a 32-bit of time-stamping signal to be outputted simultaneously with the sampling pulses. These latches are initialised either directly by the RTC or through the Signal Processor Module as described below.

The RTC has two connections to the satellite receiver, an RS422 serial interface and a miniature BNC connection. It receives accurate date and time information via the serial link. It also uses this serial link to initialise and set up the receiver. Through the BNC connection, the satellite receiver provides the DSM with precision 1 pps (pulse per second). A precision time/counter in the RTC locks onto the GPS 1 pps and is used to synchronise the sampling processes of the CHART III system to an accuracy of 1 μs. The accurate date and time information can be redirected to the P2 interface where they are outputted to the P2 bus concurrently with the sampling signals. This time information is also latched inside the Event Trigger Interface to time-tag the captured events. This date and time information is also transferred to the DSP which then broadcasts it to the rest of the CHART III system through the MIX baseboard.

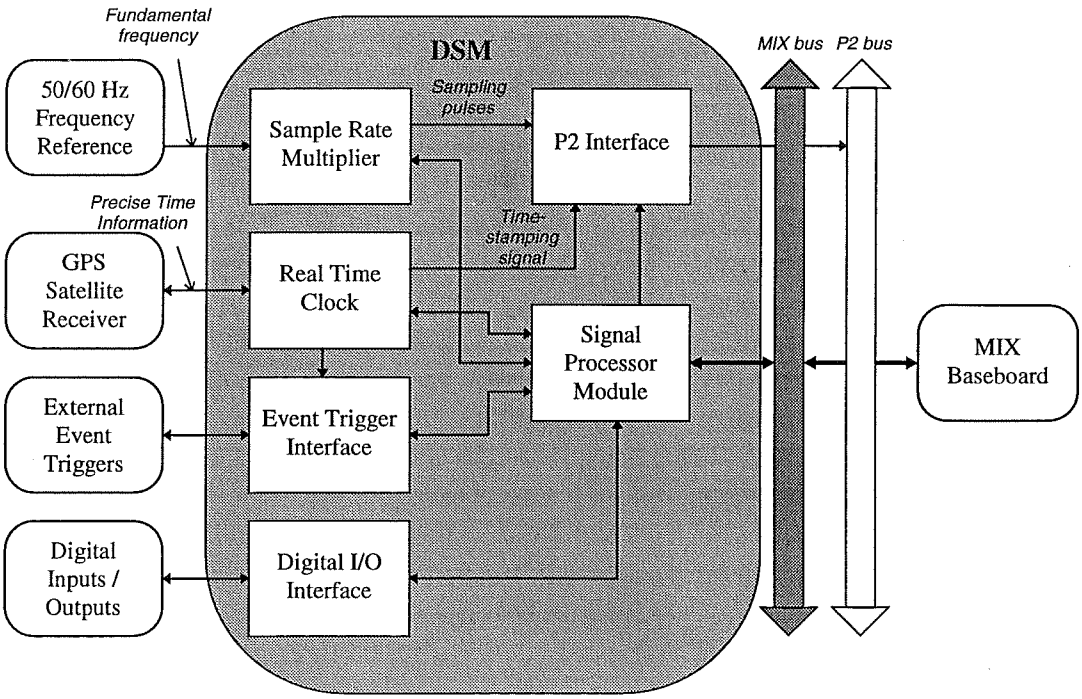


Figure 7-10: DSM block diagram

Besides the main functions described above, the DSM is also designed to provide three channels of precision event trigger capability with fibre optic interface and another three channels with opto-isolated inputs. Each event trigger can be time-stamped with an accuracy

of 1 μs with reference to the precision 1 pps. One potential application of such an event trigger is to capture the time of arrival of a transient wavefront for the location of HVDC line faults [Dewe *et al.*, 1993]. Furthermore, digital I/O ports are also designed into the DSM to provide additional means for inputting status information and outputting control signals.

The Signal Processor Module controls and sets up the operation of the DSM. It consists of Texas Instrument TMS320C31 DSP with local RAM and a DPR (dual port RAM) mechanism facilitating the communication with the MIX baseboard. The DPR is memory mapped into the memory space of the MIX baseboard through the MIX bus, enabling the transfer of data and time information to the baseboard and for downloading of DSM software programs into the DSP local memory. The Signal Processor Module also has direct access to the latches in the P2 interface. This capability facilitates the transfer of any application specific information from the DSM to all DAPM's concurrently with the sampling pulses.

7.5.6 Data Acquisition and Processing Module

The Data Acquisition and Processing Module (DAPM) is the number crunching unit of the system. It receives digitised samples from the RDCM and performs computationally intensive manipulations of the samples. The sampling and timing signals needed for the sampling process can be obtained from the DSM via the P2 bus or internally generated using the internal timers within the DAPM. For synchronised sampling, the sampling signals from the DSM must be used. The sampling signal is transmitted to the RDCM via a fibre optic link. In return, the DAPM receives digitised data and this data is then processed in the Signal Processor Module before being dispatched to the rest of the system through the MIX baseboard.

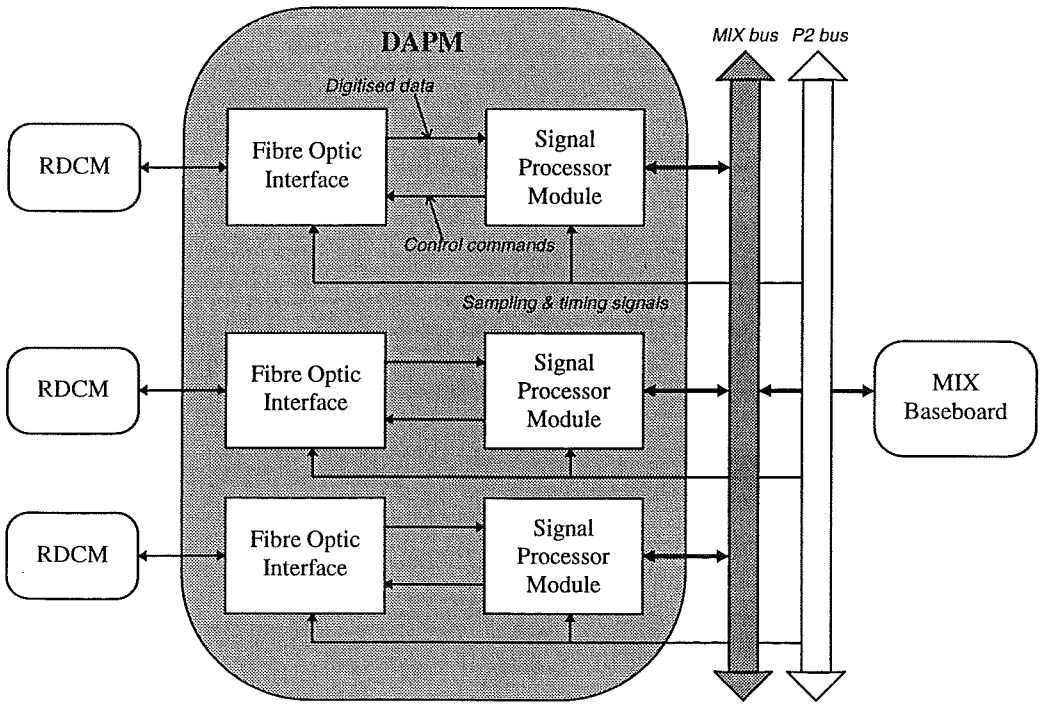


Figure 7-11: DAPM block diagram

The DAPM is designed as a MIX I/O module, and each DAPM consists of three separate identical data processing units. Each unit is made up of a Fibre Optic Interface and a Signal

Processor Module. The Signal Processor Module consists of a Texas Instrument TMS320C31 DSP operating at 32 MHz with its own private RAM and DPR. The DPR in each of the three Signal Processor Modules within a single DAPM are mapped onto different locations of the MIX baseboard memory space. This enables the MIX baseboard to separately identify each of the Signal Processor Modules, facilitating independent setup and control of the operation of individual modules. This also enables the loading of different software binaries into each of the modules allowing different algorithms to be used on a single DAPM.

The Fibre Optic Interface is designed as a full duplex software-configuration interface, providing the DAPM with the capability of interfacing with a wide variety of RDCM modules. This interface uses the TAXI mechanism [TAXI, 1992], and its operation is controlled by the corresponding Signal Processor Module. It has four modes of data transfer, providing a selectable 8, 16, 24 or 32 bit wide data path. These modes are selected and configured through software, and the transmitter and the receiver can be set up independently and differently. The interface is able to handle data transfer rate of up to 32 Mbits/s. This translates to 1M samples per second for 32-bit wide transfer and 2 M samples per second for 16-bit transfer. With this flexible fibre optic interface, the DAPM can be used with different kinds of RDCM as long as the RDCM fibre optic interface complies with the TAXI protocol and is able to operate in one of the aforementioned modes. To interface with the Type A RDCM described in section 7.4.2, the DAPM Fibre Optic Interface is configured to 8-bit transmit and 16-bit receive data transfer modes.

7.6 Control And Display Unit

The main function of Control And Display Unit (CADU) is to provide a user-friendly graphical user interface for the display of acquired data, and for setting up and controlling the operation of the CHART III system. Currently it is based on an IBM-compatible personal computer with custom designed software running on Microsoft Windows For Workgroup version 3.11. The main system requirements of the CADU is a personal computer capable of running Microsoft Windows 3.11 and having an Ethernet network connection. Although the existing CADU software is designed as a Microsoft Windows application, future CADU's may be implemented on other platforms such as X-Windows running on a Unix workstation.

The functions of the CADU are twofold. It interfaces with the user, issuing control and setup commands to the PPU for configuring each of the processors in the PPU. Secondly, it obtains data from the PPU through the HUB processor and provides a graphical presentation of the acquired information to the user. The CADU interface is made up of a series of "windows" each performing a specific function. Figure 7-12 shows the user interface provided by the current version of CADU. It consists of several functional windows contained within the Main window. The Main window uses the Microsoft Windows MDI (Multiple Document Interface) feature to accommodate the multiple functional windows within a single application. The Configuration window shows the list of connected PPU's and the hierarchy of processors contained in each of the PPUs. There are several types of display windows available in current system as shown in the figure. They are designed for the display of time domain data, harmonic data, measured fundamental frequency and the current time received from the GPS receiver. Besides these four types of displays, the flexible software architecture described latter in Chapter 8 allows custom displays to be incorporated into the system without any modification required to the CADU itself. This capability facilitates the development of specialised displays for customised applications implemented in the DAPM.

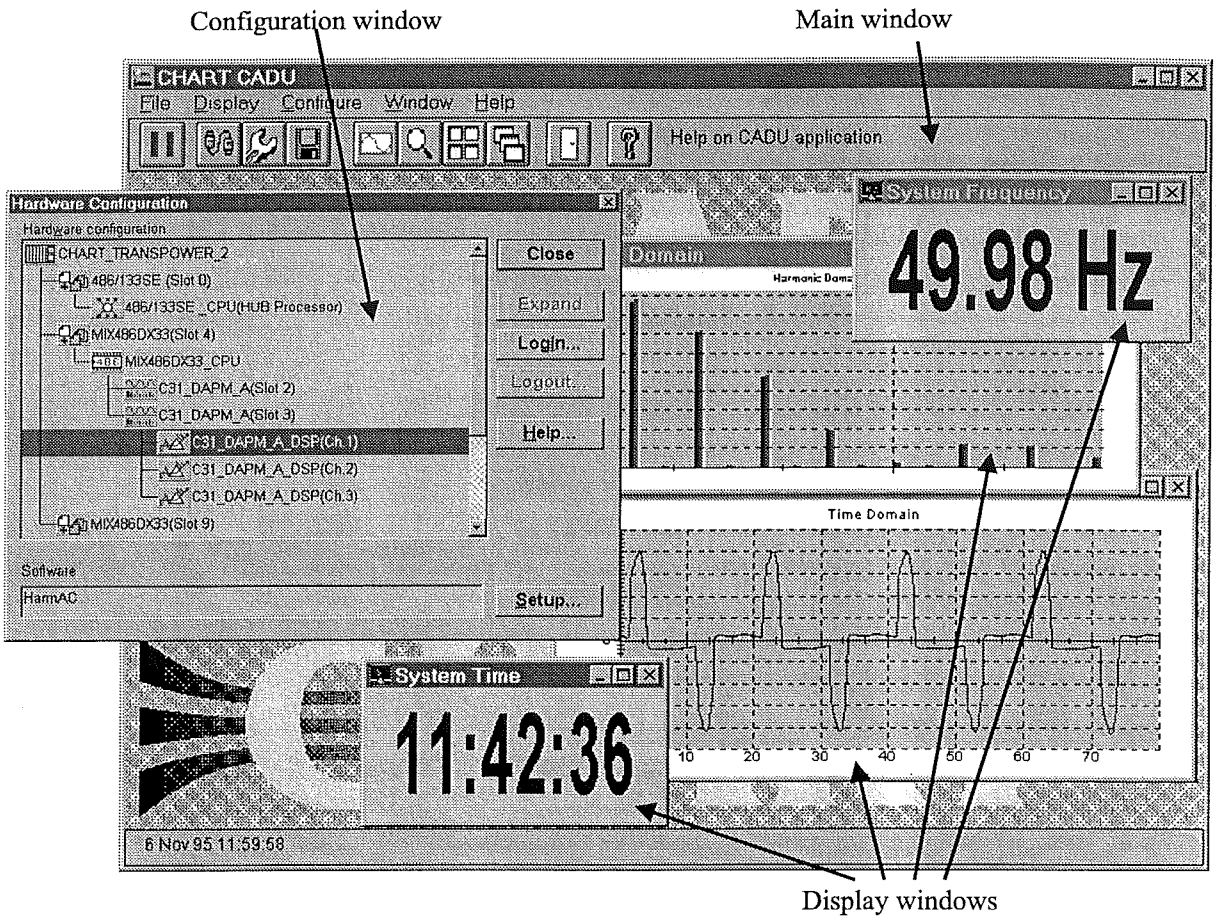


Figure 7-12: A typical CADU interface

Besides these interfaces, there are also interfaces for setting up the data storage to be undertaken by the HUB processor in the PPU, and for setting up and controlling the operation of each of the processors within the PPU. Through these user interfaces, users are provided with the capability of deciding on the processing algorithms to be used in the processors and the data that are to be stored.

Within an Ethernet network, multiple HUB processors (and hence PPU's) and multiple CADU's can interact with each other freely. A single CADU can be connected to multiple HUB processors simultaneously. Similarly, a HUB processor is capable of servicing multiple CADU's simultaneously. However, only one of the connected CADU's is able to control the operation and to change the settings of the PPU, while others operate solely as display workstations with no control functions.

The CADU is a fully compatible Microsoft Windows application and therefore can be used concurrently with a wide variety of commercial analysis and publishing tools. The graphical displays of the CADU can be transferred into other programs for further analysis or for the preparation of documents and reports. Moreover, the CADU includes a dedicated software program to assist in sifting through megabytes of acquired data for analysis purposes. This program allows the data to be presented in different formats and styles, and can be dynamically extended to include new types of displays.

7.7 Expansion and upgrade opportunity

The CHART III system has been designed with the intent of maximum flexibility for future upgrades and expansions. The modular architecture has greatly reduced the complications customarily encountered in the upgrade and expansion processes. Furthermore, the flexible architecture of the software has decoupled one processor from another enabling them to be upgraded separately. This enables the expansions of the CHART III system to be undertaken in manageable stages. Moreover, the system has been designed so that new components can operate alongside existing components within the same system. Industrial standard hardware and software are used wherever it deems applicable to minimise the dependency on any proprietary component.

The first and most obvious expansion opportunity is to develop different types of RDCM for various applications. The RDCM would have to be equipped with fibre optic interface compatible with that of DAPM in order to transfer the data to the PPU for processing. Alternately, a new DAPM may be developed. The new DAPM can be designed as MIX module interfaces with the rest of the system through the MIX baseboard or as a MBII module with direct connection to the Multibus II iPSB backplane. The latter design enables the direct communication between the new DAPM and the HUB processor. Likewise, a new version of DSM may be developed with more advance features.

Besides developing new CHART III custom hardware, the general purpose computers used in the CHART III system can also be upgraded with minimum effort. The MIX baseboard and HUB processor used in the PPU are 486 based SBC's and can be upgraded to their Pentium counterparts. This would improve the throughput and processing bandwidth of the system. Lastly, the personal computer used in the CADU can be upgraded to any better-spec machine, as long as the software requirements are met and the machine has an Ethernet interface. The CADU can be a normal desktop computer or a portable laptop computer.

7.8 Conclusion

The architecture of a flexible data acquisition has been described. The design of this CHART III system is based on a modular distributed processing structure. Although the hardware structure possesses the potential for a wide range of uses, the software must be designed so that the full capability of the system can be utilised. The architecture of such a software design is presented in the next chapter.

Chapter 8

CHART III Virtual Operating System

8.1 Introduction

It has been suggested that the modular structure of the CHART III hardware possesses the potential for use in a multitude of applications. However, this potential can not be achieved without comparable software design to exploit the flexible capabilities provided by the system. This situation is clearly depicted in the CHART II system where the software design was oriented solely towards power system harmonic measurements, even though the distributed hardware structure is capable of undertaking other functions. This chapter describes the software architecture of the CHART III system which completes the transformation of the CHART system from a dedicated harmonic analysis instrument to a flexible multipurpose data acquisition system.

The philosophy behind a flexible data acquisition can be described using the block diagram in Figure 8-1. It consists of two sets of modules interconnected by a single general interface module. A flexible data acquisition system should allow customised algorithms and applications to be implemented at the front end near the source of the data, while at the same time enabling specialised control, setup and display interfaces to be used at the user end. This functionality has to be achieved without the need for the user to implement complicated and tedious interfaces between the two sets. Therefore, the general interface module should

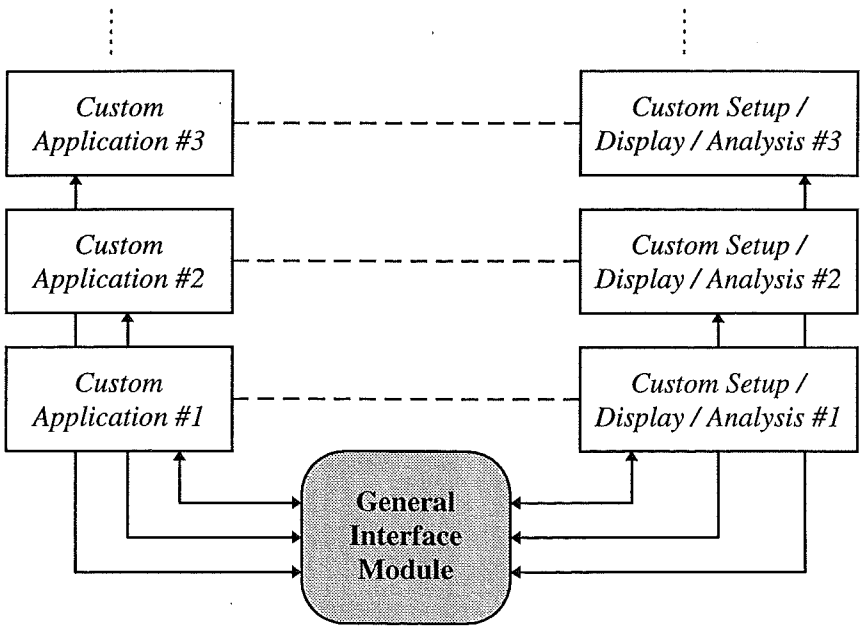


Figure 8-1: Philosophy of a flexible data acquisition system

undertake the transfer of control and setup commands from the user interface to the front end processors where the algorithm is implemented, and in return the transportation of acquired and processed data back to the user for display and analysis. Furthermore, a customised application is most likely to be associated with certain custom-designed control, setup or display interfaces. Such transparent links have to be included in the design of the general interface module so that different customised applications and user interfaces can be utilised in a single system concurrently.

Besides providing the capability of adapting to different kinds of applications, it would be advantageous if commonly used functions in the data acquisition system such as the data storage are included in the design. These features would greatly reduce the time and effort required on the part of user to carry out the measurement. The functions provided would also have to be able to accommodate different kinds of data samples resulting from the wide ranging types of applications.

The CHART III system, like many data acquisition systems, possesses several custom built hardware modules integrated with some commercially available components. Specific hardware interfaces would have to be designed to communicate with the custom built components while those commercial components are usually provided with proprietary operating systems, easing the integration process. Therefore, the CHART III software design includes the functional capability of interfacing to two different groups of components.

The functions needed by the CHART III software very much resemble those of a typical operating system. Therefore, the CHART III software architecture is generally referred to as the CHART III Virtual Operating System. An overview of this virtual operating system is presented in the following section. The organisation of several key items reflecting the role played by each part of the virtual operating system is then described. It is followed by detail descriptions of individual components within the virtual operating system.

8.2 Overview of CHART III virtual operating system

An operating system is generally defined as the interface between the human user and the computing hardware. Its main function is to provide a user friendly method for instructing the computer to perform certain task. It can be regarded as three separate parts comprising a user interface, a command interpreter and the implementation of the instruction. A command or instruction is issued via the user interface and is decoded by the command interpreter. The decoded instruction tells the operating system what task is to be conducted. This command can be an operating system command or an instruction to activate a particular application. The operating system then proceeds to carry out the instruction and if necessary it can fetch the program binary from secondary storage devices.

The CHART III virtual operating system closely resembles the operating system terminology outlined above. The distributed nature of the hardware provides user with the choice of deciding what application is to be activated similar to the invocation process mentioned above. It also provides transparent interfaces to the hardware devices and the commands issued through the user friendly CADU are decoded and carried out in similar manner to a normal operating system. However, there are several compelling differences between this virtual operating system and the better known operating systems. Firstly, this virtual operating system is made up of several parts with each part manifesting itself on different hardware and on different platforms. The current version of CHART III system uses Texas Instrument TMS320C31 DSP and Intel 486 processors, and runs on Intel iRMX real time multitasking

operating system and MSDOS and Windows. Secondly, it is not a true fully self-contained operating system as it only provides interfaces to the CHART III custom-made hardware while making use of the commercial proprietary operating system such as the iRMX to gain access to the other devices such as the 486 CPU on the MIX baseboard and the hard disk connected to the HUB processor. Lastly, the main difference which significantly distinguishes this virtual operating system from the normal operating system and at the same time makes it a true data acquisition system is its transparent handling of the flow of data samples from the front ends to the storage and display interfaces.

In order make CHART III a multi purpose system, the software design is divided into two layers namely the Application Layer and the Virtual Operating Layer or System as shown in Figure 8-2. The virtual operating layer or system provides interfaces to the custom hardware devices and to the commercial operating systems. This arrangement eliminates the need for the user to learn about the hardware design and the different kinds of operating systems used in the system. It allows the users to introduce their algorithms or applications into the system with minimum effort. The virtual operating layer or system transmits the control and setup commands and the data acquired from the hardware devices to the application, and in return receives the responses to the control and setup commands, and the processed data. Through this virtual layer or system, the user-definable application is able to access the hardware devices and to make use of the services provided by the normal operating systems.

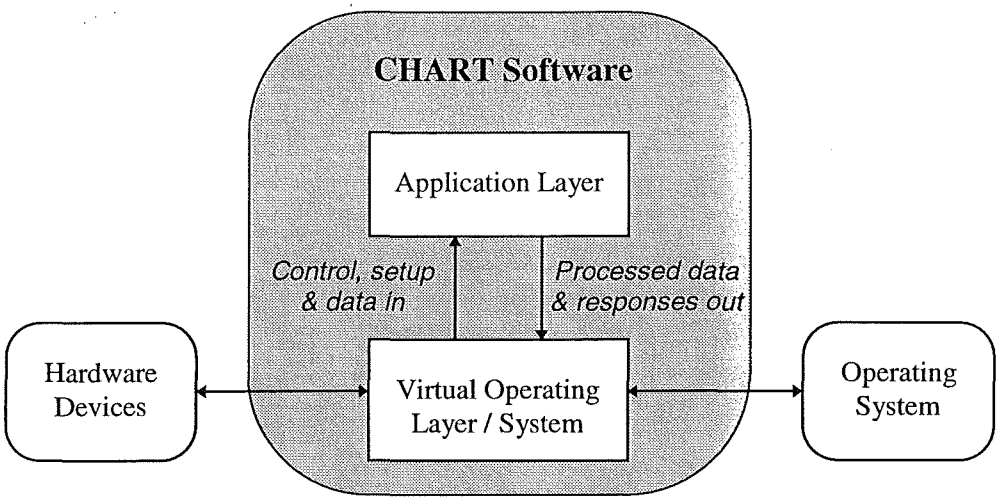


Figure 8-2: CHART III Software Application and Operating Layers

The CHART III virtual operating system is divided into five different parts corresponding to each of the five hardware items within the system as shown in Figure 8-3. In the DAPM and DSM, it is referred to as the operating layer instead of operating system because the operating layer binaries are combined with the application binaries to generate a single DAPM or DSM program. The prime purpose of these layers is to provide the DAPM and DSM application with transparent hardware interfaces to the connected RDCM, GPS receiver and fundamental frequency reference source respectively. On the other hand, in the MIX baseboard, the operating system and the application are separate programs. The MIX baseboard and the HUB virtual operating system both operate on top of the Intel iRMX real time multitasking operating system. The iRMX operating system provides them with access to the hardware devices including the CPU, the hard disk and the iPSB bus, and it also manages the time slices for the running of these operating systems. The CADU virtual operating system sits on top of the MSDOS and Windows operating system. It is basically a Windows program

providing a standard user friendly interface for the entry of commands and instructions. A transparent layer has also being designed to enable the utilisation of third party commercial display and analysis tools and also to allow new custom display and analysis software to be incorporated into the system with minimum effort.

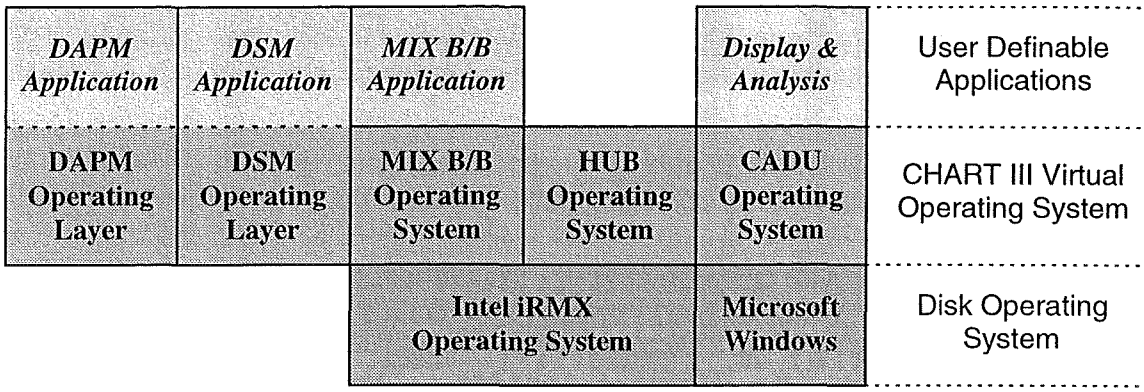


Figure 8-3: Overview of CHART III Virtual Operating System

8.3 Organisation of the virtual operating system

This section details the organisation of the various major elements within the virtual operating system. The properties of these elements determine how the entire virtual operating system will function and how it will be presented to the end users. The basis for these elements is the need to manage the two major flows of information in the operation of the CHART III system as depicted in Figure 8-4. Control commands and setup parameters entered by the user at the CADU have to be transmitted to the targeted ends of the DAPM and the DSM. Application software binaries for the MIX baseboard, DAPM and DSM have to be retrieved from the HUB processor hard disk and loaded into the respective units. On the other hand, processed data samples from the DAPM and timing signals from the DSM are transferred from these front end units to the user interface of the CADU through the HUB processor which also carries out the storage of the data samples.

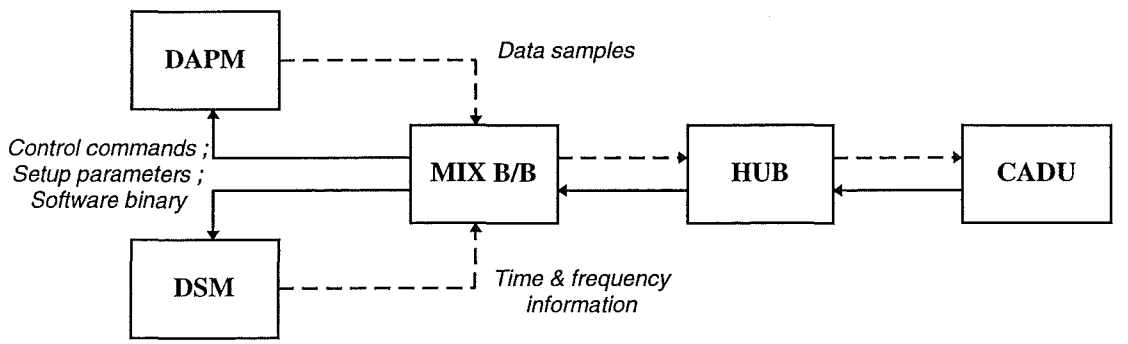


Figure 8-4: The CHART III system data flow diagram

The major elements described in this section include the organisation of the hardware items with a special addressing scheme so that each of the individual items can be identified and accessed either separately or collectively as a group. This is followed by the description of the organisation of the commands used in the virtual operating system and the manner by which the setup parameters or arguments are passed to the front end application software. Various

details, required by the virtual operating system in order to coordinate the loading and activation of the application software, are also illustrated in the following subsections. Unique to this virtual operating system is the management of the flow of processed samples from the front ends to the user interface. The concept of these schemes and their benefits are also described.

8.3.1 Organisation of hardware items

In order to achieve full benefits from the modular structure of the system, a unique hierarchy addressing scheme has been established to reference individual hardware items. The concept is based on the notion that only the processor can be used to implement computations while a board is simply an entity for accommodating a single or multiple processors. The addressing scheme consists of four levels of board and processor numbers as shown in Figure 8-5. It begins from within the PPU and expands to cover all the data processing capabilities between the front end A/D convertors and the user interface. Several CHART III hardware items are included in the figure to illustrate the use of this scheme.

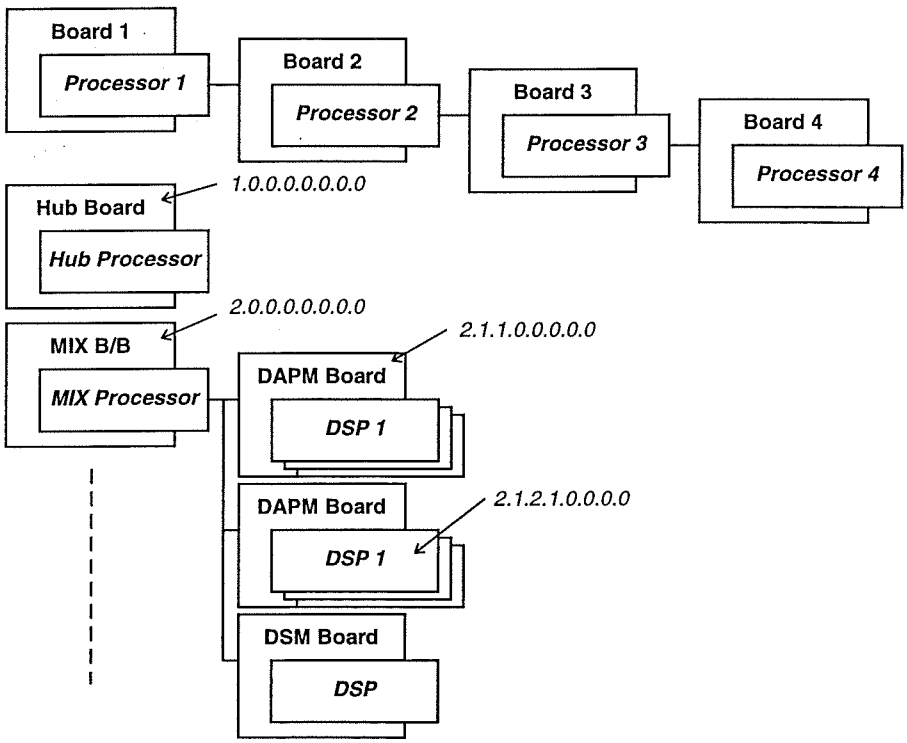


Figure 8-5: Hierarchy addressing scheme used in CHART III

The first set of items along the left side of the diagram designated as Board 1 are the Multibus II boards connected directly to the iPSB backplane of the PPU. In the current version of CHART III, they are made up of the HUB processor board and a series of MIX baseboards. Processors 1 are the CPU or processor onboard the Multibus II board which possess the data processing capability. These processors may be connected to a series of boards such as the 486 CPU onboard the MIX baseboard is connected to several DAPM and DSM boards. These daughter boards of Processor 1 are designated as Board 2 in the second level of the addressing scheme. The processors onboard Board 2 such as the TMS320C31 DSP onboard the DAPM and DSM are referred to as Processor 2 which may in turn connected to another series of boards designated as Board 3 in this scheme. Board 3 and Processor 3 are not used in the

current version of CHART III but will be used to refer to the new multi-channel RDCM which contains a DSP. In this tree-like manner, the addressing scheme expands itself to include new data processing boards and processors.

With this addressing scheme, the HUB processor board and the MIX baseboard are referenced by the addresses of 1.0.0.0.0.0.0.0 and 2.0.0.0.0.0.0.0 respectively, while the first DSP on the second DAPM board is identified by the address of 2.1.2.1.0.0.0.0. This scheme can also be used to reference several items simultaneously such as to load all the DSP's on the first DAPM. In the above example, the load-software command to all the DSP's on the first DAPM will contain the address of 2.1.1.0.0.0.0.0 with processor 2 number equal to 0 implying all the processors residing on that DAPM. This hierarchy addressing technique enables each of the processors in the system to be identified individually and therefore to be configured independent of other processors.

8.3.2 Organisation of operating system commands

The commands used in the virtual operating system are divided into three categories: system commands, generic commands and software dependent commands. The system commands are used to set up the environment within the virtual operating system. This includes the setting up of the data storage processes, the data back up and retrieval procedures and the maintenance of the various databases used in the system. Special graphical user interfaces are designed on the CADU for the entry of these commands and the HUB processor is usually the target processor for such commands. These commands will be interpreted and the requested action conducted within the perimeter of the virtual operating system.

The generic family of commands are designed specifically for coordinating the operation of

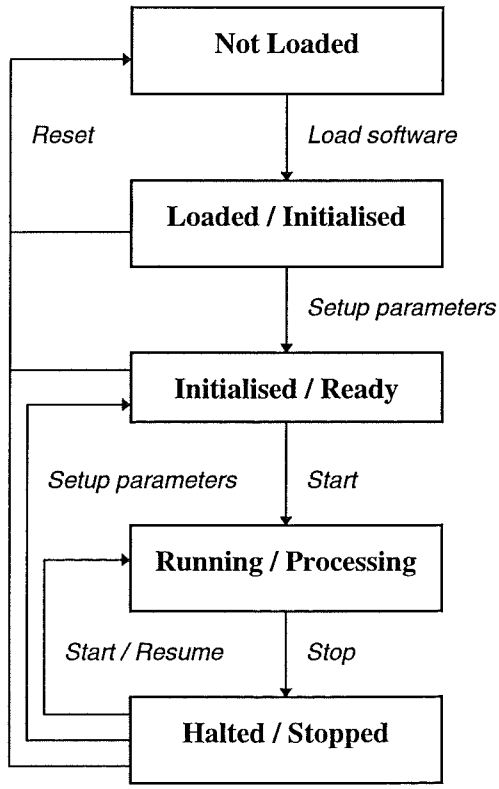


Figure 8-6: Flow diagram of the activation of CHART III application

the application software. It consists of the reset, load-software, start and stop commands. Figure 8-6 shows the flow diagram of these commands in activating a typical application software. Upon power up, the hardware device which is regarded as a processor within the system is in the not-loaded state and the load-software command is used to initiate the loading of a particular software binary into the memory. The loaded software is then initialised with a list of setup parameters specific to this application. The details of how the virtual operating system handles a flexible number and types of setup parameters are described in the next section. The initialised application is then activated with the start command. While in the running or processing state, the stop command can be used to halt the program. Operation can then be resumed using the start command, or reinitialised with new setup parameters or reset back to the not-loaded state. These generic commands provide a systematic way of controlling the operation of each individual application software from the remote end user interface of CADU. Generic user interfaces are implemented in the CADU for the entry of these commands, but there are also provisions for custom setup user interfaces to issue these instructions.

Finally, the software dependent commands are commands specific to a particular application software and their functions and meanings are known only to the application software itself. Therefore, each application software has it own list of software dependent commands designed specifically for its purposes. A standard convention has been established for these commands whereby they are enumerated within the virtual operating system and text strings are used to reference these commands at the user interface. Activating a software dependent command at the user interface is achieved by sending the targeted processor a message containing a flag indicating that this is a software dependent command, and with the command enumeration and any associated details. This method enables new commands to be defined as needed by the ever evolving family of application software.

Through these three levels of command, the end users are provided with the ability to establish the environment of the system and the complete control over the operation and behaviour of each of the applications. With the system commands, the common functions provided in the data acquisition system is set up according to the user's requirements. The generic commands provide the user with the choice of algorithms to be used in the system. Lastly, an unlimited number of software dependent commands provide the users with the opportunity to implement and control their customised applications without any constraints.

8.3.3 Organisation of application setup parameters

The function of the setup parameters is similar to the input arguments or switches used with normal operating system commands. Its prime purpose is to supply the application with the information needed for its operation. Each application with its own purposes requires different information and is most likely to have a different set of setup parameters. A current measuring application will have the burden resistor value as one of its parameters, whereas a voltage measuring one may have the system nominal voltage as its parameter. The values of these parameters are entered at the user interface and are transmitted to the front end processors where the applications are functioning.

In the CHART III virtual operating system, a series of data formats such as 16-bit integer and 32-bit floating point are compiled into a single list for use as the setup parameters. Each setup parameter can be a single element or an array of a certain data format and is referenced at the user interface with a text string. This fixed configuration of data formats enables a series of standard user interfaces to be designed for the entry of parameter values. It also facilitates the

implementation of the External Data Representation (XDR) scheme used for the transfer of information across different hardware on different platforms. This technique has simplified the interaction between the MSDOS and Windows environment of the CADU and the iRMX operating system used in the HUB processor. It also simplifies the conversion between the data formats used in the Intel 486 CPU and the Texas TMS320C31 DSP.

8.3.4 Organisation of processed data samples

The flexibility provided by the proposed system which allows the use of different application software and variants of front end RDCM's means that the resultant data packets will have different structures. Therefore, a procedure has to be established for the virtual operating system to perform data collection, distribution and storage. The design of this procedure is based on the preposition that the virtual operating system does not carry out any data processing, and hence does not have to know the format of the data packets. All the information it needs relates to its duty of collecting, distributing and storing the data packets. This information includes the length of the individual data packet, its description in the form of a text string, and the frequency with which it has to be collected, distributed and stored.

The list of data formats used for the setup parameters is also applied to the data samples. This enables data samples to be transferred in their most appropriate form, convenient for display or analysis purposes as determined by the customised applications and hardware devices. Moreover it also enables the acquired data to be maintained in the hardware native format, preserving the measurement accuracy and resolution. Furthermore, the use of the aforementioned XDR scheme has facilitated the conversion of these formats across different platforms, allowing the data to be analysed with tools running on different platforms.

The virtual operating system also allows several items of subsidiary importance to be kept with the data packets. These details are oriented to the needs of the display and analysis program. They include several text strings denoting the type of data packet, the x and y axes units and the colour to be used when displaying the data. The text string representing the type of data packet is used to associate the data samples outputted by a particular application to certain display interfaces at the CADU. In this way, users are provided with total freedom in defining their own data packet format according to the needs of their applications.

Two modes of data transfer are supported by the system, the continuous and the burst transfer modes. In the continuous mode, the above details have to be provided to the rest of the operating system before the transmission can commence. This is to allow appropriate buffers to be created to accommodate the data transmission. On the other hand, in the burst mode, these details are transmitted together with the data in a single packet. Burst transfer mode is primarily used in the surveillance type of applications, where a pre-defined number of pre-event and post-event data samples are captured and transmitted as a single packet.

8.3.5 Organisation of application software

The organisation of the application software is one of the major features in CHART III virtual operating system which make the system unique compared to other commercial systems. It not only enables the system to be set up for differing applications but also allows new applications to be easily incorporated within the CHART framework.

All CHART application software has to be designed according to the organisation of the commands, setup parameters and data samples as described in the preceding sections. Its

operation has to conform with the flow diagram of Figure 8-6 and the setup parameters are defined using the fixed list of data formats. The processed data samples also have to be organised as discussed above and are represented using the fixed list of data formats.

A database has been created on the HUB processor's hard disk to keep the details of the application software. This application software database is arranged according to the type of hardware the software is designed for. The current version of DAPM with three TMS320C31 DSP will have its own list of application software. The DSM similarly has its own list. Within the database is the information needed by the virtual operating system to coordinate the loading, initialisation and activation of the program. This information includes file pointers indicating the location of the software binaries in the hard disk, the details of the software dependent commands and the details of each of the setup parameters needed for the correct functioning of the application. Similarly, text strings are used in the virtual operating system when referring to individual application software.

The information contained in this database is presented to the user through the CADU according to the hardware item selected by the user. From these details, the user can decide what program is to be used on the device and control the program's operation using the various commands and setup parameters. The virtual operating system also provides users with the facilities to maintain the database and for installing new application software into the database.

8.4 Description of the virtual operating system

This section describes in detail the five sections making up the virtual operating system. They are the DAPM and DSM operating layers, the MIX baseboard, HUB processor and CADU operating systems. The design of these operating layers and systems is oriented around the functions to be performed by each of the processors. The DSP processors onboard the DAPM are responsible for processing the acquired data. The main function of the DSM is to generate the sampling and time-stamping signals. The MIX baseboard on the other hand is responsible for transferring the processed data from the DAPM and the date and time from the DSM to the rest of the system. Furthermore, there are the collection, distribution and storage of the data, the centralised control functions performed by the HUB processor, and finally the user interfacing duties of the CADU. These operating layers and systems are described individually in the following sections.

8.4.1 DAPM operating layer

The function of the DAPM is to perform the computationally intensive manipulations on the data samples. It has three hardware connections which are the fibre optic link to the RDCM, the P2 bus to the DSM and the MIX bus to the MIX baseboard. Figure 8-7 shows the layout of the DAPM operating layer which consists of a Main module and three hardware interface modules to the RDCM, DSM and MIX baseboard. The purposes of the DAPM operating layer are to:

- control the operation of the RDCM,
- receive the sampling signals from the DSM and relay them to the RDCM,
- collect data samples from the RDCM via a fibre optic link,
- time-stamp the received raw data and deliver it to the application for processing, and
- handle the transmission of the processed data to the MIX baseboard.

The RDCM module contains functions specific to the particular type of RDCM. The current version of RDCM includes automatic calibration, dynamic gain ranging and the conversion from 16-bit fixed point number output by the A/D convertor in the RDCM to the 32-bit floating point format used in the DSP. This module also sets up the DAPM fibre optic interface to operate in 8-bit transmit and 16-bit receive data transfer mode. The received data samples are transferred to the Main module.

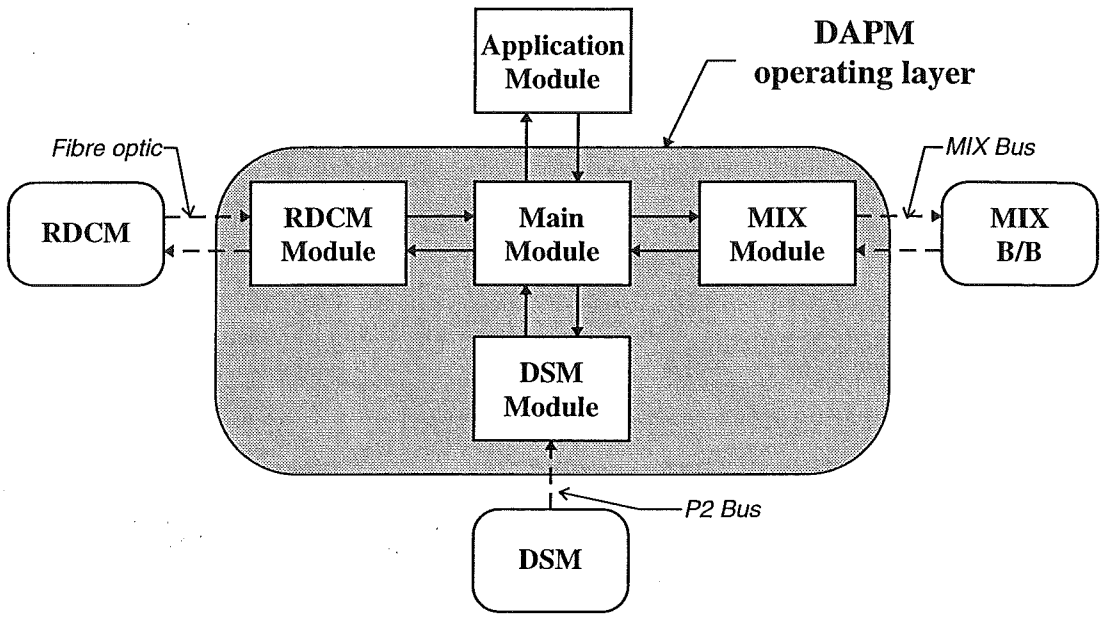


Figure 8-7: DAPM operating layer

In the Main module, the samples are time-stamped with the accurate 32-bit time obtained from the DSM module before passing the data to the Application module. The DSM module acts as the heart of the system outputting the sampling pulses needed by the RDCM and generating interrupts to initiate the collection, processing and dispatching of the data samples. It counts the number of sampling pulses outputted to the Main module and generates an interrupt when a certain pre-defined number of pulses is reached. This number is initialised by the Application module through the Main module and usually corresponds to the end of a fundamental cycle. The generated interrupt is first used by the RDCM module to collect the list of data samples from its front end buffers and which is then passed over to the Main module. After time-stamping the data, it is forwarded to the Application module for calculation and the processed data is then returned to the Main module. Through the MIX module, this processed data is transmitted to the MIX baseboard and then to the rest of the system. The DSM module is also capable of generating sampling pulses using the DSP internal timer when the DSM is not available.

The Main module also receives the control commands and the setup parameters via the MIX module and coordinates the implementation of these instructions. Software dependent commands and setup parameters are passed onto the Application module and the responses are relayed back to the MIX baseboard via the MIX module. Besides guiding the traffic through the MIX bus , the MIX module also performs the necessary conversion between the data formats used in the TMS320C31 DSP and those used in the Intel 486 CPU on the iRMX platform.

With the operating layer providing all the necessary functions to drive the DSP and its interfaces, the design of the application is concentrated on the numerical algorithm used to process the data samples. Therefore, the task of designing a new DAPM software has been reduced to the definition of several procedures. These procedures constitute the Application module and are *app_init* which is executed immediately after the program is loaded, *app_calculate* called to process the data, *app_command* and *app_setup* called when the Main module receives software dependent control commands and setup parameters respectively. Through these procedures, the application can alter the operation of both the DSP and the RDCM according to the requirements of the application.

There are three DSP contained in a single DAPM. The DAPM operating layer described in this section refers to the software module executed by each individual DSP. This operating layer will be common to all the DSP's if they are connected to similar types of RDCM. However, since each DSP can be configured independently, the application module may consist of different algorithms even though similar RDCM and DAPM operating layers are used. With new versions of RDCM, different RDCM modules would need to be designed to include various functions specific to these new RDCM's.

8.4.2 DSM operating layer

The DSM operating layer of Figure 8-8 has a similar structure to the DAPM layer except that the front end hardware interfaces are different. The RTC module is responsible for the operation of the Real Time Clock onboard the DSM. It interfaces with the GPS satellite receiver through a RS422 serial interface and also receives the precision 1 pps (pulse per second) via a miniature coax cable. The RS422 serial interface is used to initialise the GPS receiver and in return the RTC module receives the accurate date and time information. Besides using this date and time information to adjust the internal Real Time Clock, the assembled timing information is sent to the Main module. In the absence of the GPS receiver or when the receiver fails to generate the timing signals, the RTC module maintains the time by driving a voltage controlled crystal oscillator.

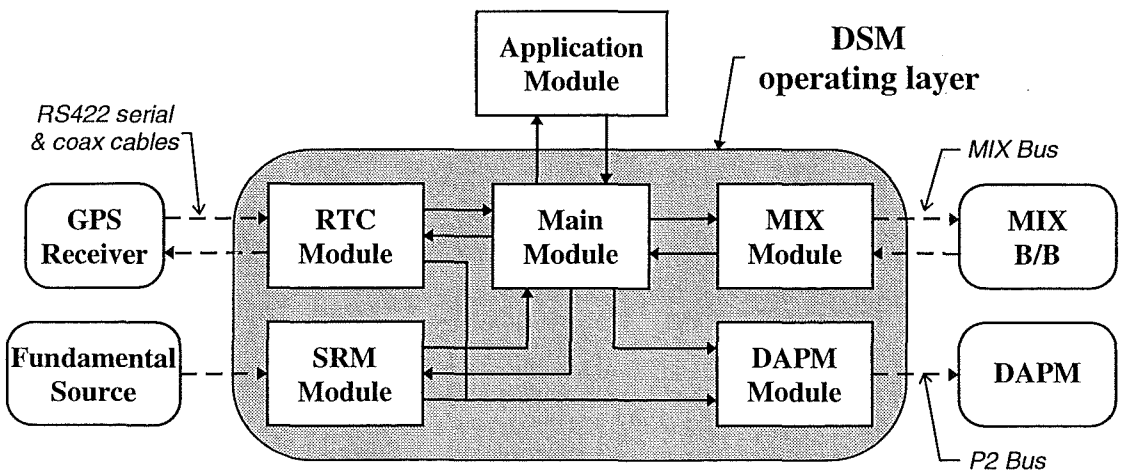


Figure 8-8: DSM operating layer

The SRM module controls the operation of the Sample Rate Multiplier which has the function of generating sampling pulses. Through a zero crossing detection circuitry, it calculates the fundamental frequency and the generation of the sampling pulses can be

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referenced to this measured fundamental frequency. This technique enables coherent sampling of the data, commonly used for harmonic analysis as it minimises the frequency overlapping effect that results from the FFT computation, and therefore removes the need to window the data samples before undertaking the frequency transformation. The measured fundamental frequency is passed onto the Main module while the sampling pulses are sent to the DAPM through the DAPM module and via the P2 bus. Depending on the Application module, this fundamental frequency information can be dispatched to the rest of the system through the MIX module.

The Main module collects the accurate date and time from the RTC module and the fundamental frequency from the SRM module, and passes them to the Application module. Depending on the initialisation undertaken by the application, this time and fundamental frequency information can be dispatched to the rest of the CHART system. The Application module consists of a series of procedures as in the DAPM and, through the Main module, the application can determine how the sampling signals are to be generated and what 32-bit information is to be outputted together with the sampling pulses to the DAPM. The DAPM module is responsible for dispatching the sampling and time-stamping signals to the P2 bus. Lastly, the MIX module in the DSM operating layer is identical to that of DAPM operating layer. It provides transparent connection between the MIX baseboard and the DSP in the DSM.

8.4.3 MIX baseboard virtual operating system

The main function of the MIX baseboard is to coordinate the operation of the DAPM and DSM while performing a limited amount of data processing. The MIX baseboard virtual operating system is built using the multitasking features of the iRMX operating system. Although not shown in Figure 8-9, the iRMX operating system forms a framework around the perimeter of the MIX baseboard virtual operating system providing access to the various hardware and software resources.

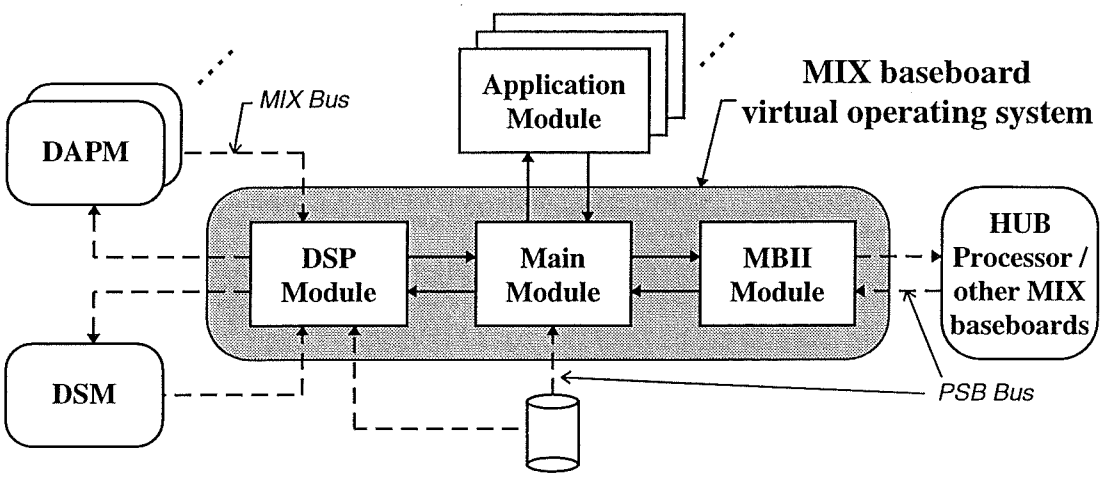

Figure 8-9: MIX baseboard virtual operating system

The MIX baseboard virtual operating system is made up of the DSP module, the Main module and the MBII module as shown in Figure 8-9. The DSP module performs a series of identical tasks, each maintaining a line of communication with a particular DSP on the DAPM or DSM. The DAPM and DSM program binaries are stored in the HUB processor

hard disk, and these individual tasks make use of the iRMX operating system commands to retrieve the binaries through the iPSB bus. They also use the iRMX commands to load the binaries onto the DSP via the MIX bus. The Main module is a task controlling the data transfer from the DSP to the HUB processor, and also to and from the applications. The applications consist of separate iRMX programs which are dynamically loaded and activated by the Main module according to the commands received from the HUB processor. There is no limit to the number of applications and the only determining factor is the amount of remaining processing power after all other chores have been completed. The applications communicate with the Main module using the message passing scheme provided by the iRMX operating system.

Lastly, the MBII module also taps into the message passing scheme of the iRMX on the Multibus II bus system and maintains the communication between this particular baseboard with the HUB processor and other baseboards. It contains a full duplex communication with the HUB processor receiving control and setup commands, and sending data samples, status and command responses in the opposite direction. Besides that, it has a simplex communication path with other MIX baseboards which is used to broadcast the date and time information. As there is only one DSM in the CHART III system providing the time information, this signal has to be distributed to other MIX baseboards which may need the information to time-stamp the processed data.

8.4.4 HUB processor virtual operating system

The HUB processor acts as the general manager of the CHART III system. It is the central collection and redistribution point of the system and is also where the data samples are stored. There is no Application module in the HUB processor and the virtual operating system is dedicated to the coordination of the operation of other units within the system. Similarly to the MIX baseboard virtual operating system, it is built with various features provided by the iRMX real time multitasking operating system. Figure 8-10 shows that the HUB processor virtual operating system consists of five modules; these are the SBC (Single Board Computer) module, Main module, Network module, Database module and Storage module.

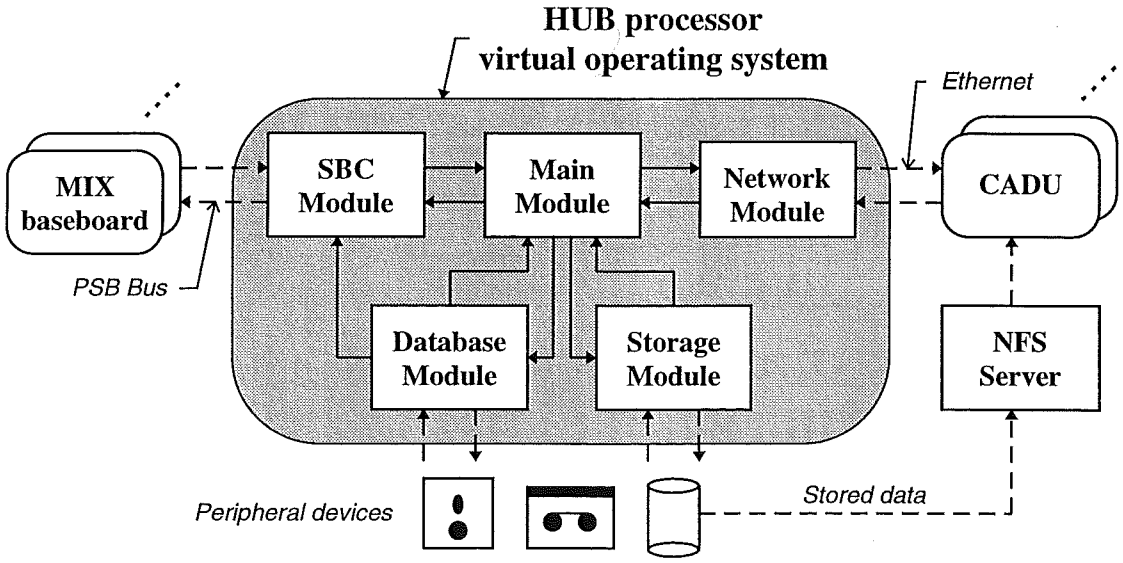

Figure 8-10: HUB processor virtual operating system

The SBC module consists of a series of iRMX jobs with each job being responsible for a single SBC attached to the iPSB backplane. These jobs are dynamically loaded according to the type of SBC being detected by the SBC module on the iPSB backplane. In the existing version of CHART III, the MIX baseboard is the only SBC and hence this module contains only the job used for interacting with the MIX baseboard. The software binaries of these jobs are kept in a database residing in the HUB processor hard disk. Therefore, a new SBC can be integrated into the system by developing a new interface job and adding it into the database, without the need to modify any of the existing software.

On the other side of the HUB processor, the Network module interfaces with the CADU through the Ethernet network. A connection based networking protocol called TCP/IP (Transmission Control Protocol / Internet Protocol) is used to transparently maintain this line of communication between them. The Network module is capable of handling multiple CADU connections simultaneously. It also performs a form of XDR (External Data Representation) to facilitate the transfer of information across the different platforms of CADU and HUB processor. In this version, both HUB and CADU run on Intel processors and therefore, their byte ordering and data formats are similar, allowing an optimised version of XDR to be implemented. The advantage of having XDR is to decouple the HUB processor from the CADU and vice versa, hence allowing future HUB processor or CADU hardware changes without major ramifications. The Main module functions as the system command interpreter and acts on the command as required. It also maintains the flow of commands and data in between the CADU and the front ends.

The Database module consists of functions used for maintaining four databases: these arethe User Database, SBC Database, Project Database and Application Software Database. The User Database contains the usernames and passwords for the CHART users and their privileges. Connections from the CADU to the HUB processor have to be validated with these usernames and passwords before being granted access to the data or control setup functions. SBC Database keeps software binaries of the jobs interfacing with each type of SBC as mentioned above. The Project Database stores details of the system setup allowing the same setup to be employed in the future. This capability not only reduces the time and effort in the setup process, but also minimises the risk of error introduced by the elaborate manual setup process. The database can maintain an unlimited number of projects and each project can be easily called up from the CADU. The Application Software Database contains the lists of application programs that can be used on DAPM, DSM and the MIX baseboard. It also contains the details of the software dependent control commands and the setup parameters. These lists of application software are transferred to the CADU for user selection and the corresponding details inform the CADU how the application can be configured and controlled. This database can be extended to accommodate new hardware devices.

Finally, the Storage module provides the Main module with a plain interface to the peripheral devices for data storage and backup purposes. The setup of the storage is carried out from the CADU and through the HUB processor's Main and Network modules. The stored data files are kept in the HUB processor's hard disk and are made available to the CADU through the NFS (Network File System) server which is part of the iRMX operating system.

8.4.5 CADU virtual operating system

The CADU is the user interface of the virtual operating system. The functions of this virtual operating system are two folds. Firstly, it provides user friendly interface for the entry of the commands specific to this system, and the various details needed to set up and maintain the

operation of the system. Secondly, it presents a systematic interface for the use of different kinds of displays and customised setup interfaces. It also facilitates the use of third party analysis and reporting tools.

Figure 8-11 shows the block diagram of this CADU virtual operating system. The Network module communicates with the HUB processor and performs the XDR conversion. The received data packets are transferred to the Data module which then dispatches them to each of the real time display windows. The Data module presents a common interface to all the display windows, enabling various kinds of displays to be developed for the presentation of data in varying styles and formats. The Control and Setup module consists of user interfaces for selecting the application software to be implemented by the processors in the system. There are also generic user interfaces for configuring the application software through the setup parameters and for the invocation of the system, generic and software dependent commands. It also provides a facility to accommodate custom-designed user interfaces for setting up a particular application. Lastly, the Storage module acts on the data files made accessible by the NFS client and allows both customised and commercial analysis and reporting tools to be used on the stored data. It is also capable of converting the data into various industrial formats including the comma-delimited ASCII text formats.

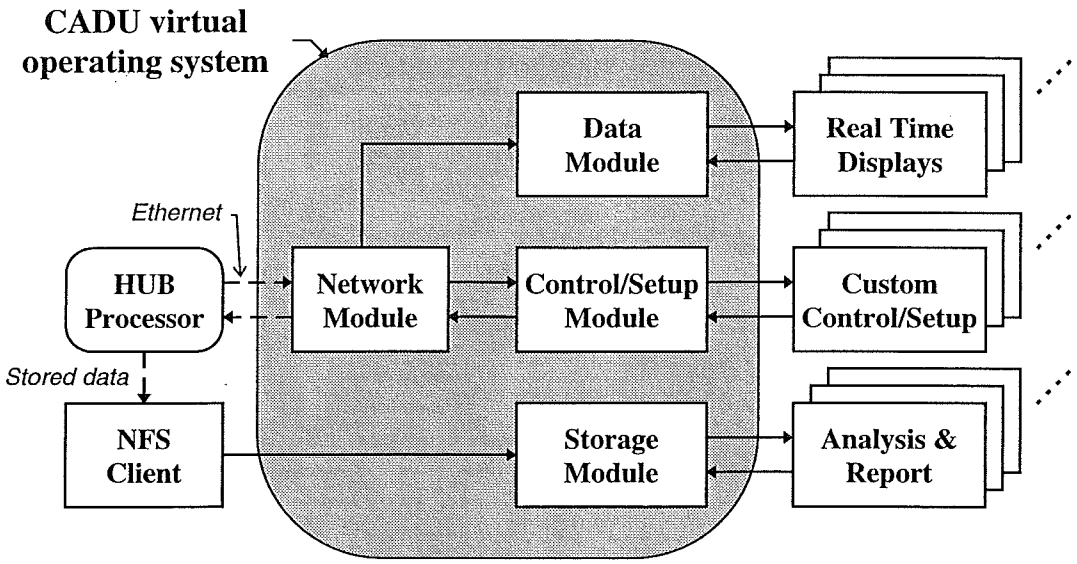

Figure 8-11: CADU virtual operating system

8.5 Conclusion

The CHART system which is a proven data acquisition system dedicated to the measurement of harmonics in power system has been transformed into a flexible multi purpose system suitable for all kinds of analysis and research uses. Its unmatched capability of continuous data processing in real time and accurate time referencing can be extended to other applications beside harmonic measurements. This has been achieved through sound software architecture in the form of a virtual operating system.

With the virtual operating system, new algorithms and computation techniques can be easily tested with existing hardware devices since new software can be easily designed and incorporated within the perimeter of the system. Furthermore, with the modular design of the virtual operating system, new hardware devices can be connected to the system for testing and

development purposes. This extension feature will reduce the time, effort and cost required in developing new devices since the rudimentary software and hardware are already provided.

The system has been designed to achieve maximum flexibility while keeping the amount of software coding to the minimum. This has been achieved by using third party software drivers and tools. As a result, the data output format is not limited to just hard copies as in most commercial systems but includes various industrial formats allowing commercial tools to be utilised. This approach is further enhanced by the use of the Windows environment in the CADU, thus making available the abundant supply of compatible third party tools provided in that environment.

Most of the concepts applied in this design are not new and may have been partly utilised in other systems. However, in this system, the various techniques are brought together to achieve a unique and powerful, yet flexible data acquisition system. The main objective of this architecture is to keep the design as simple as possible. More complicated designs may seemingly provide more attractive features, but they tend to be inflexible and unable to carry out applications outside the intended circle of operations. Finally, clear interfaces and boundaries have been carefully defined throughout the virtual operating system, enabling individual parts of the system to be modified and improved without adverse effects on other parts. This not only facilitates the continuous development of the virtual operating system itself, but also minimises the impact that changes or upgrades of the hardware devices may bring to the rest of the system.

Chapter 9

Applications of CHART III System

9.1 Introduction

In November 1995, there have been two great opportunities for demonstrating the data acquisition flexibility provided by the CHART III system. They are the two field measurements referred to as the Benmore Islanded Convertor Test and the New Zealand South Island Synchronised Test. Both tests have widely differing requirements and objectives, and therefore provide an excellent opportunity to illustrate the capability of the CHART III system. Both of these tests are described in this chapter with specific attention to the application of the CHART III system in achieving the objectives of the tests.

9.2 Overview of the Benmore Islanded Convertor Test

The recently upgraded New Zealand HVDC link between Benmore in the South Island and Haywards in the North Island is made up of a rather unique configuration, with a combination of mercury-arc and thyristor valves. The Benmore convertor station consists of two poles as shown in Figure 9-1, of which Pole 1 comprises two paralleled mercury-arc valve 12-pulse convertors and Pole 2 a thyristor valve 12-pulse convertor. There are six generators at the Benmore hydro station each capable of generating 112.5MW. The generators feed the Pole 1 convertors through convertor transformers and, normally, the six generators are divided equally among the two parallel convertor branches. However, there is provision for shifting one generator to the other half of the pole to achieve a 2 and 4 generator configuration. Under normal operation, Pole 1A and 1B are operated concurrently with the dc current shared equally between the convertors.

Through the interconnecting transformers T2 and T5, the generators and Pole 1 convertors are connected to the rest of the New Zealand South Island system, including the Pole 2 convertor. The 220kV system forms the backbone of the South Island electrical network and the Benmore Pole 2 convertor draws power directly from this system. There are two banks of harmonic filters connected to the tertiary windings of the interconnecting transformers and additional harmonic filters are installed at the 220kV bus to supplement the extra harmonic filtering requirement from the Pole 2 convertor. During normal operating conditions, the scheme is always operated with the harmonic filters in service and the convertor system is always connected to the rest of South Island electrical network. A form of power modulation is implemented in the HVDC scheme to maintain the fundamental frequency in both South Island and North Island ac networks.

In November 1995, the need to decommission transformer T5 from service for routine maintenance resulted in a unique operating condition for Pole 1B. First, the entire Pole 1B convertor including the ac system connected to it would be islanded, resulting in a form of group connection. Secondly, the Pole 1B convertor would be operated without any harmonic

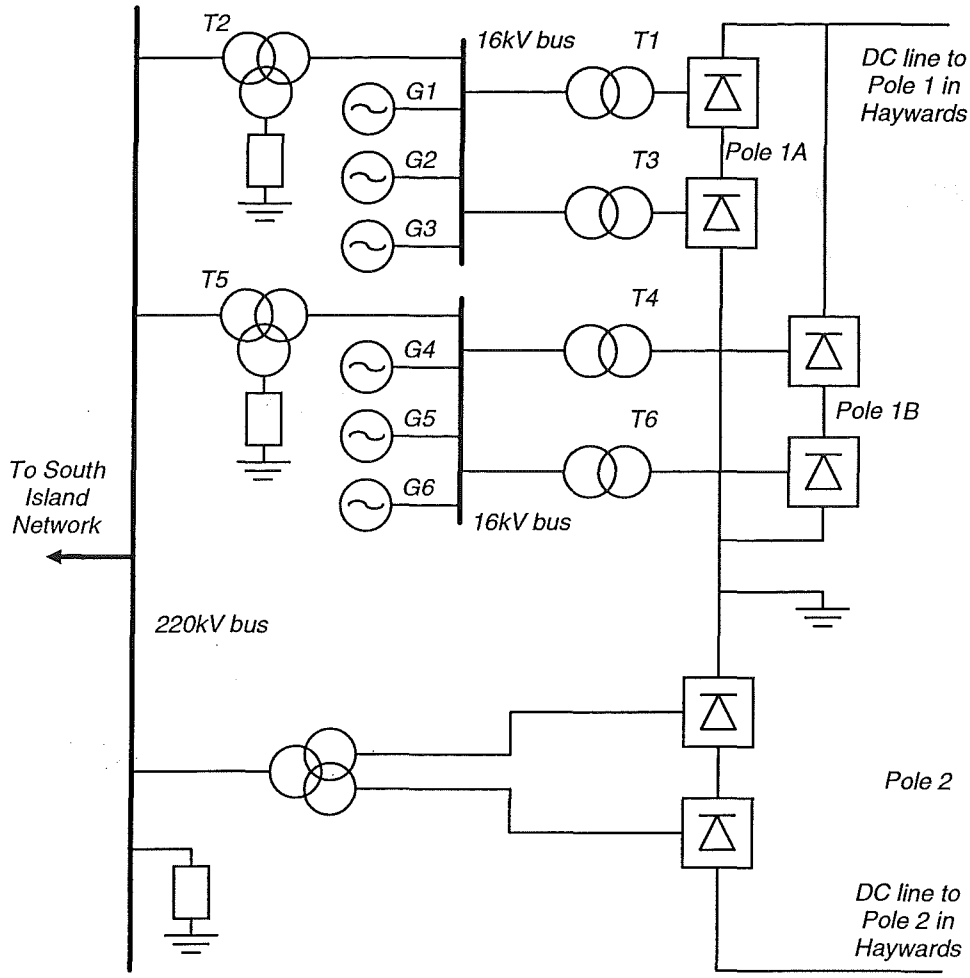

Figure 9-1: Benmore HVDC convertor station

filters on its ac side, thus subjecting the generators to greater harmonic distortions than under normal operation conditions. Moreover, the fundamental frequency of the islanded network could deviate from the nominal 50Hz depending on the dc load and the amount of generation. This operating condition provided a great opportunity to gather various field measurements to validate the computer simulation models developed at the University of Canterbury.

The absence of harmonic filters and ac network allows the harmonic characteristics of the generator to be evaluated. The research activity at the university has particular interest in the effect of the generator rotor angle on the harmonic conversion process caused by the salient pole synchronous machines. The rotor angle affects the phase shifts in the cross-couplings between harmonic frequencies and this effect is particularly important in a group connection due to the close proximity between the generators and convertors, and the absence of harmonic filters. Accurate modeling of this effect is required in order to achieve a correct salient generator model in the harmonic domain. By measuring the generator currents and voltages, it should be possible to work out this effect and the results can be used to validate and improve the generator model.

An accurate representation of the HVDC convertor in the harmonic domain is vital for the analysis of harmonic interaction of the convertor with the connected ac network. A recently developed model [Smith *et al.*, 1995] has endeavoured to predict the generation of non-characteristic harmonics by the convertor as a result of commutating voltage distortions and

unbalance in the ac system impedance. However, it is difficult to verify this harmonic domain model if the convertor is operated under normal conditions, due to uncertainties in the ac system impedance and the measurement of very low harmonics when the harmonic filters are in service. The islanded scheme with group connection and without any harmonic filter offers a well defined system with relatively large harmonic distortion. The harmonic measurements in such a system should provide a more thorough validation of the convertor model and instill more confidence on the prediction of non-characteristic harmonics by the model.

In a group connected HVDC scheme, there is a strong harmonic interaction between the generators and the convertors. A unified generator-convertor harmonic model is currently being developed and the test measurements would provide the necessary harmonic information to verify this new model in the future.

Besides capturing the waveforms needed for validation of computer models, this test provides the opportunity to illustrate some of the capabilities of CHART III described in previous chapters. These include the ability to perform alternative data processing tasks, the transparent handling of the different data formats resulting from the tests, the ability of CHART III to track the varying fundamental frequency in the islanded ac system and, its use to ensure coherent sampling.

9.3 Configuration of CHART III for the Benmore Test

Figure 9-2 shows the islanded system at the Benmore convertor station. Two CHART III units were used to provide a total of twenty-four data channels, but due to the geographical locations of some of the measurement points, only nineteen channels were used in the test. The measurements include the voltage at the 16kV bus, generator currents, convertor transformer currents, Pole 1B dc line voltage and current, and the firing angle of the Pole 1B

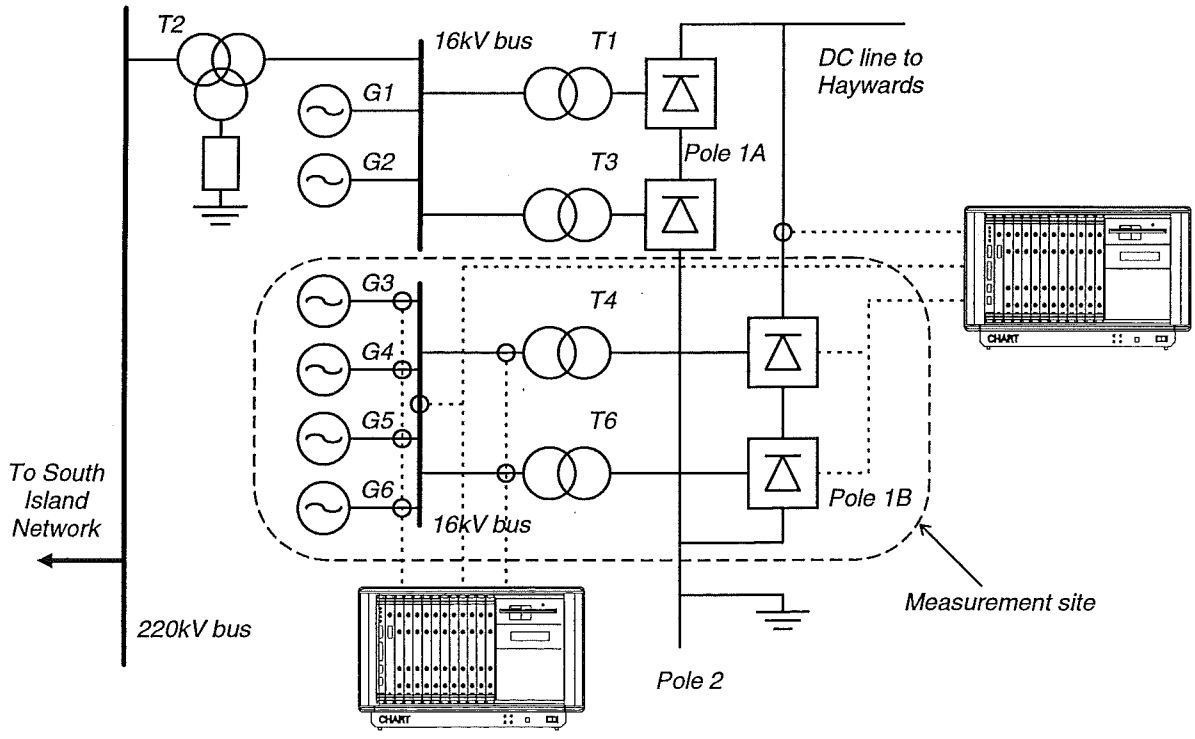

Figure 9-2: CHART measurement points in the Benmore Test

convertor. The main task of the CHART III system was to capture the time domain waveforms under different dc current and ac generation configurations. It was decided to capture two different forms of time domain data, a small number of samples per fundamental cycle over a longer period for steady state analysis and a handful of cycles of data with a much higher sampling rate for resolving the switching instants of the convertor. Therefore, the CHART III system was programmed to gather the following two sets of time domain data: 256 cycles of 128 sample points per fundamental cycle and 8 cycles with 1024 points per cycle. In addition to these two sets of data, their harmonic contents were also computed to be used for online real time display and for post processing the data after the test.

The two main parts of CHART III that need to be addressed in this test are the DSM application and the DAPM application. Figure 9-3 shows the setup of the DSM and DAPM in this test. The DSM application was originally designed for the Synchronised Test described in the latter part of this chapter and no separate DSM application was designed or needed for this test. Only a brief description is provided in this section, the full details being included in the section on the Synchronised Test.

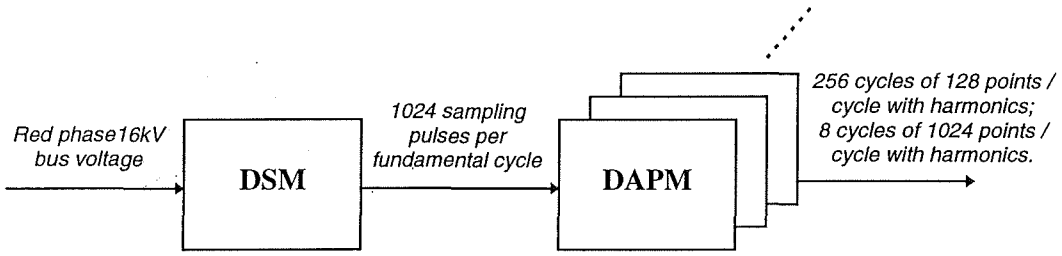

Figure 9-3: Setup of DSM and DAPM application software for the Benmore Test

The DSM is programmed to generate 1024 sampling pulses per fundamental cycle with the fundamental frequency referenced from the red phase voltage of the 16kV busbar. Adjustments are made if the fundamental frequency drifts away from its previously measured values so as to maintain exactly 1024 pulses within a single fundamental cycle throughout the measurement.

The DAPM application software is designed to operate on a cycle-by-cycle basis with 1024 samples designated as one cycle. Figure 9-4 shows how the DAPM application processes and generates the wanted data as outlined above. The numbers contained in the rectangular boxes refer to a fundamental cycle (1024 raw samples) and the computation part of the application is activated at the end of each cycle. Only the first 264 cycles of data are used to produce the wanted data and the cycle number is reset back to 1 when it reaches 3000 which corresponds to nearly one minute if the fundamental frequency remains at about 50Hz.

The first 256 cycles of time domain data are passed through a FIR filter with 8:1 decimation reducing the number of samples per cycle from 1024 to 128 points. The resultant 256 cycles of 128-point time domain data are packed in groups of 8 cycles producing a total of 32 packets. Furthermore, every 8^{th} cycle (1^{st}, 9^{th}, 17^{th}, etc.) the samples are Fourier transformed to extract their harmonic contents. The resultant harmonic packet is 102 points in length, the first 51 points taken by the magnitude of the harmonics from dc to the 50^{th}, and the rest by the phase angles. Each of these harmonic packets as well as the corresponding 8-cycle time domain data will be used for the verification of the simulation models.

The second set of data is simply the raw 1024 points per cycle time domain samples. However, the harmonic contents of this data may be useful for future analysis and thus cycles

257 to 264 are also FIR filtered and Fourier transformed to obtain the harmonics. The computed harmonic information is combined with the corresponding single-cycle time domain data to form the second set.

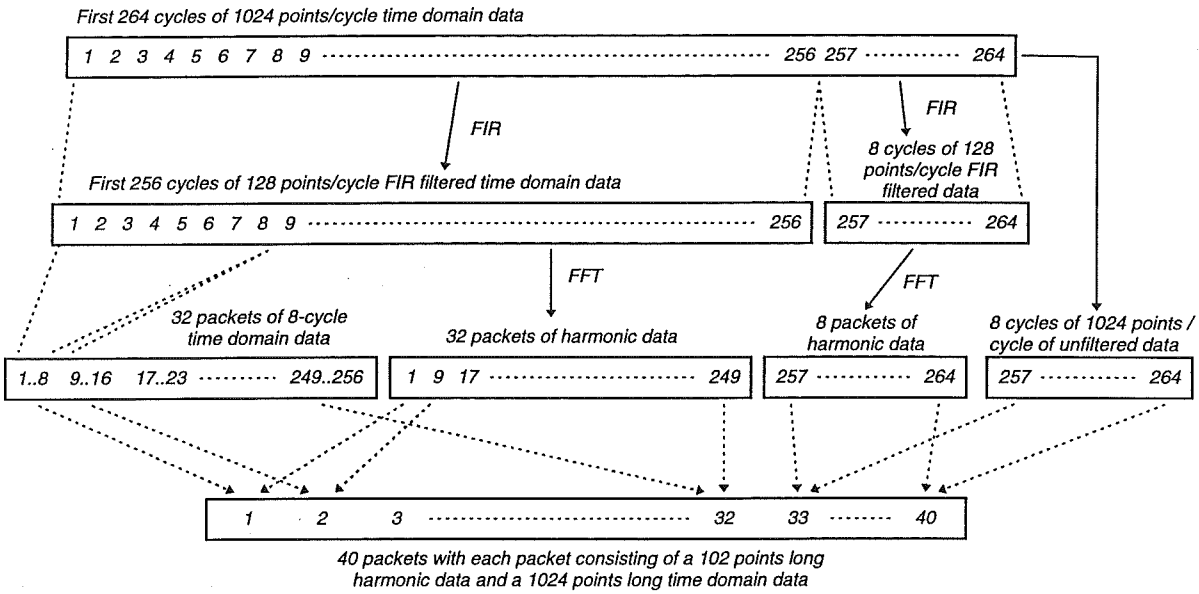

Figure 9-4: Data processing carried out by the DAPM in the Benmore Test

The acquired data has to be sampled simultaneously in all channels to be useful for verifying the simulation models. This is achieved by utilising the DSM as the sole source of sampling pulses in each CHART III unit and a synchronisation process incorporating a GPS system is employed in each unit to link the operation of the two DSM's together. The DSM application allows the dispatching of the sampling pulses to be deferred until a pre-defined time is reached. Identical starting time is set up in both DSM's and with similar time information received by the DSM's from the accurate GPS satellite system, the first sampling pulse is issued at the same instant in both units. The same red phase 16kV bus voltage is fed into both units to provide a common reference for the fundamental frequency, thereby ensuring that the sampling process in both units takes place concurrently.

9.4 Summary of the Benmore test

The test was carried out over a five hour period with the dc current and ac generation settings varied approximately every 30 minutes. This allowed several sets of data to be collected for verifying the computer simulation models under different operating conditions.

Although the DAPM application is capable of generating the intended data every 3000 cycles, approximately every minute, it was decided that there would be too much redundant information. Instead, the DAPM application was set up to generate the data every 9000 cycles corresponding to approximately every three minutes. This would produce at least three sets of data for each dc current and ac generation setting, while allowing 10 to 15 minutes for the system to settle to steady state after each configuration change.

The test was carried out successful despite an accidental tripping of Pole 1 convertor when connecting the CHART III units to the system. Changes in the dc current and ac generation were achieved smoothly, with Pole 1A convertor covering any shortfall as a result of the

variations in Pole 1B convertor. A total of over 200 Mbytes of data was recorded providing more than 24 sets of usable data with 8 different dc current and ac generation settings.

Figure 9-5 shows a selection of recorded data over a fundamental cycle at several measurement points, under a particular configuration. The generator G5 current and the

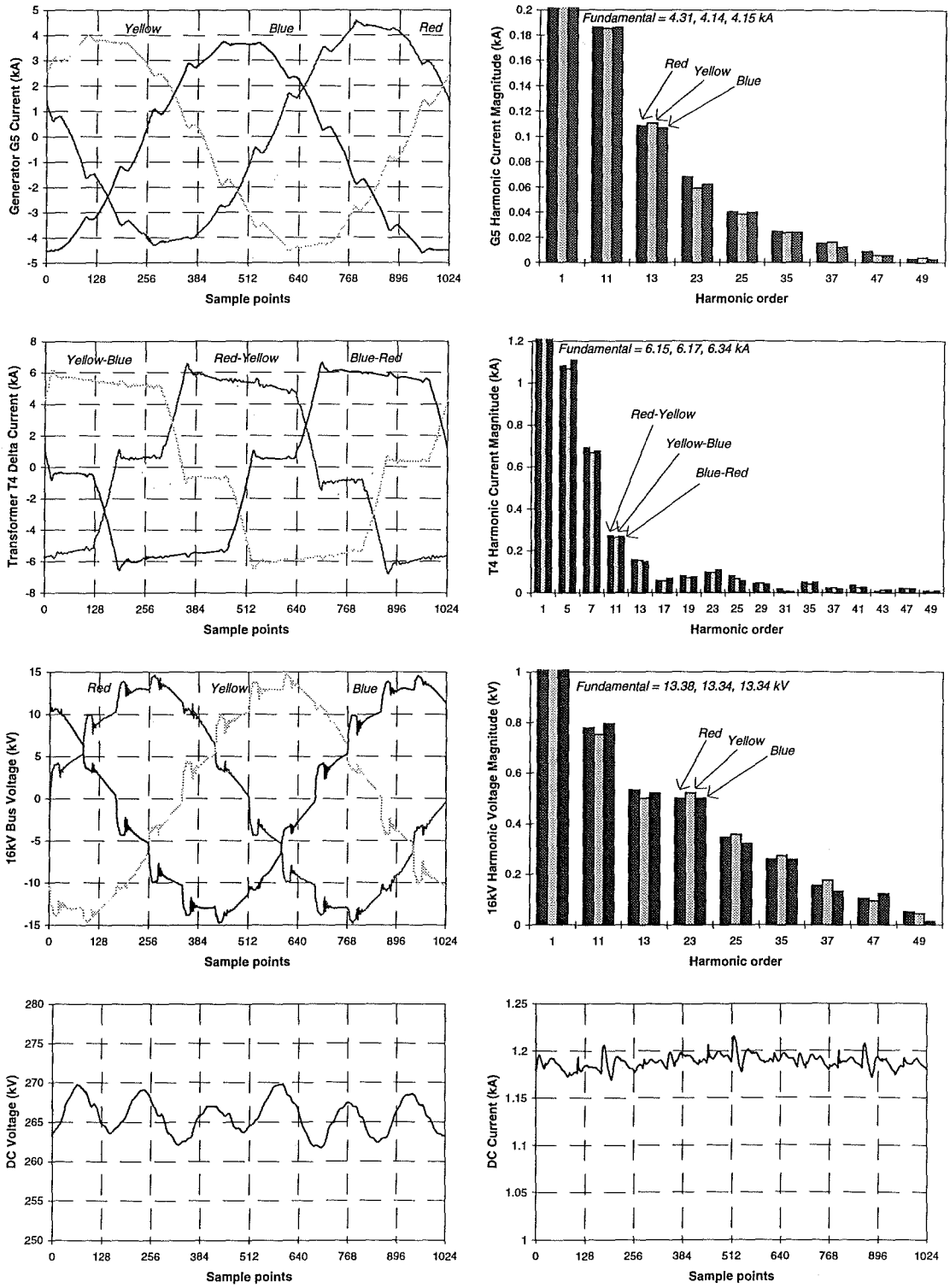

Figure 9-5: Selection of data acquired in the Benmore Islanded Convertor Test

voltage waveforms contain a substantial amount of characteristic harmonics as expected in a scheme without harmonic filters. The T4 transformer delta current shows the presence of the expected harmonics. Lastly, the presence of 6^{th} harmonic distortion is clearly evident in the dc voltage waveform as well as a considerable distortion in the dc current.

Apart from a few problems with the storing of captured data in the hard disk, the CHART III systems functioned as expected throughout the test. This test is the first CHART field measurement not directly related to the calculation of harmonics in an ac electrical power network. Although the test has demonstrated the capability of the CHART III system, the full benefit of the test will have to wait until the data is used to validate and refine the computer simulation models.

9.5 Overview of the South Island Synchronised Test

The South Island Synchronised Test was devised as the acceptance test for the two CHART III systems to be supplied to Trans Power New Zealand Limited who operates the New Zealand national grid. The test sites were chosen at the Islington substation near Christchurch and at the North Makawera substation near the southern tip of the South Island. The geographical location of the two CHART III units used in this test is shown in Figure 9-6.

Between the Islington and North Makawera substations, there are a number of hydro stations and a HVDC scheme. The distribution network at Islington has reported a substantial amount of 5^{th} harmonic distortion caused by the presence of a large number of industrial sites in Christchurch connected to this circuit. The 5^{th} harmonic current is largely absorbed by the compensation capacitors at the Islington substation. However, the capacitors are usually removed from service during light load conditions causing the 5^{th} harmonic current to flow into the 220kV transmission system. On the other hand at North Makawera, the opposite effect has been observed, with the 5^{th} harmonic current flowing from the 220kV transmission network into the distribution system. The main consumer of electrical power fed by the North Makawera substation is the aluminium smelter at Tiwai. A recently installed 5^{th} harmonic filter at Tiwai was frequently overloaded and the source of the 5^{th} harmonic current distortions was traced to the 220kV transmission system.

The first objective of the test is to find out if there is any connection between the 5^{th} harmonic problems at the Islington and North Makawera substations. If there is a relationship between the two problems, the response of the 5^{th} harmonic distortions at North Makawera to the switching of capacitors at Islington is to be identified. This required that the measurements undertaken at both sites to be synchronised as accurately as possible. The 5^{th} harmonic problems at both substations were known to vary with the daily operation of the South Island system. Therefore, the two CHART III units had to gather harmonic information of the system over a fairly long period, covering a variety of operating conditions.

9.6 Configuration of CHART III for the Synchronised Test

Figure 9-7 shows the 220kV electrical network of the South Island system. The 220kV network is the main transmission system in the South Island, providing the only electrical connection between Islington and North Makawera substations. The CHART III units were set up at both places to monitor as many as possible of the currents flowing between the 220kV transmission system and the substations.

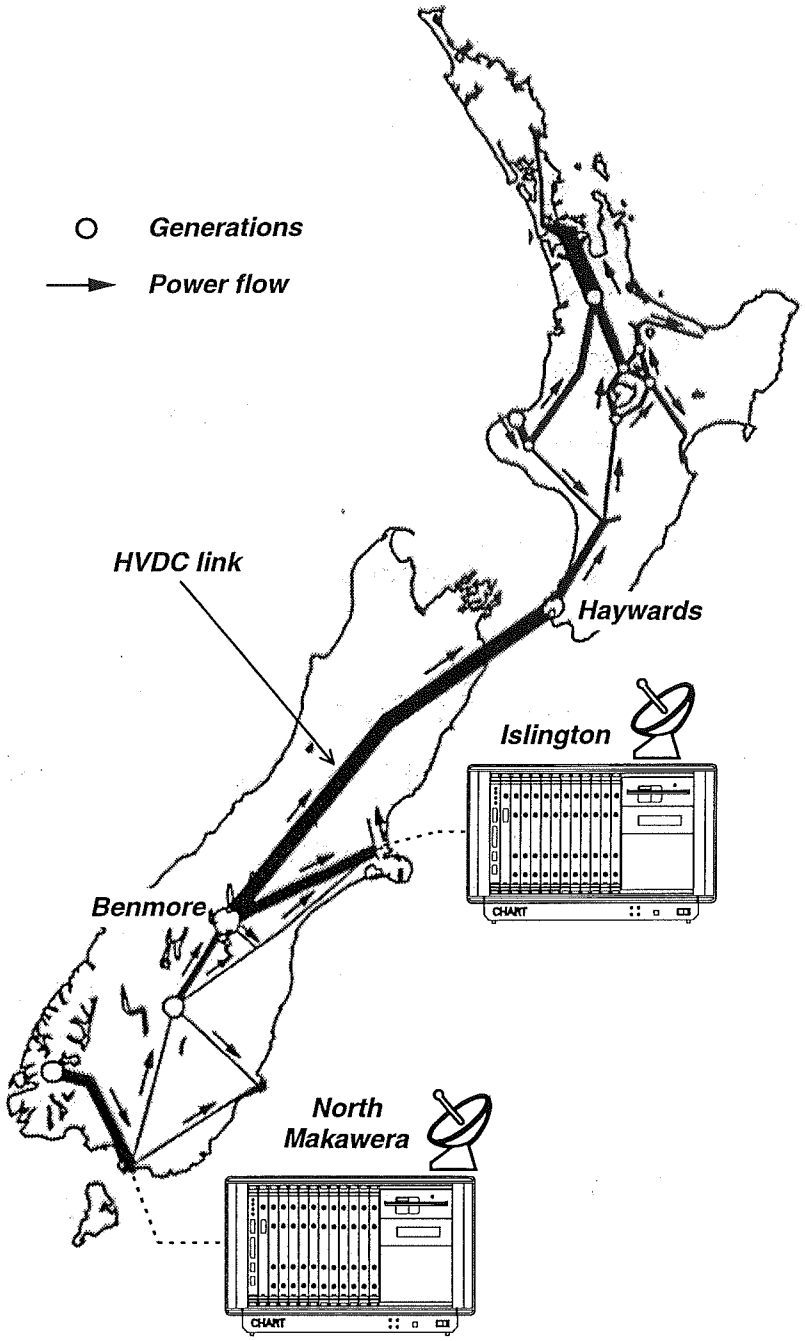

Figure 9-6: Location of CHART units in the Synchronised Test

At Islington, the two transmission lines considered to have the lowest impedance between the substation and the generating stations around Benmore are the Islington-Livingston and Islington-Timaru-Twizel lines. All three phases on these two circuits were measured. Besides measurements on the 220kV system, the voltage distortion on the 66kV bus was also monitored. The compensation capacitors are connected to the 66kV distribution circuit at Islington which are known to contain a substantial amount of 5^{th} harmonic distortion. The CHART III unit was also set up to record the current of one of the transformers (T3) interconnecting the 66kV distribution network and the 220kV transmission network.

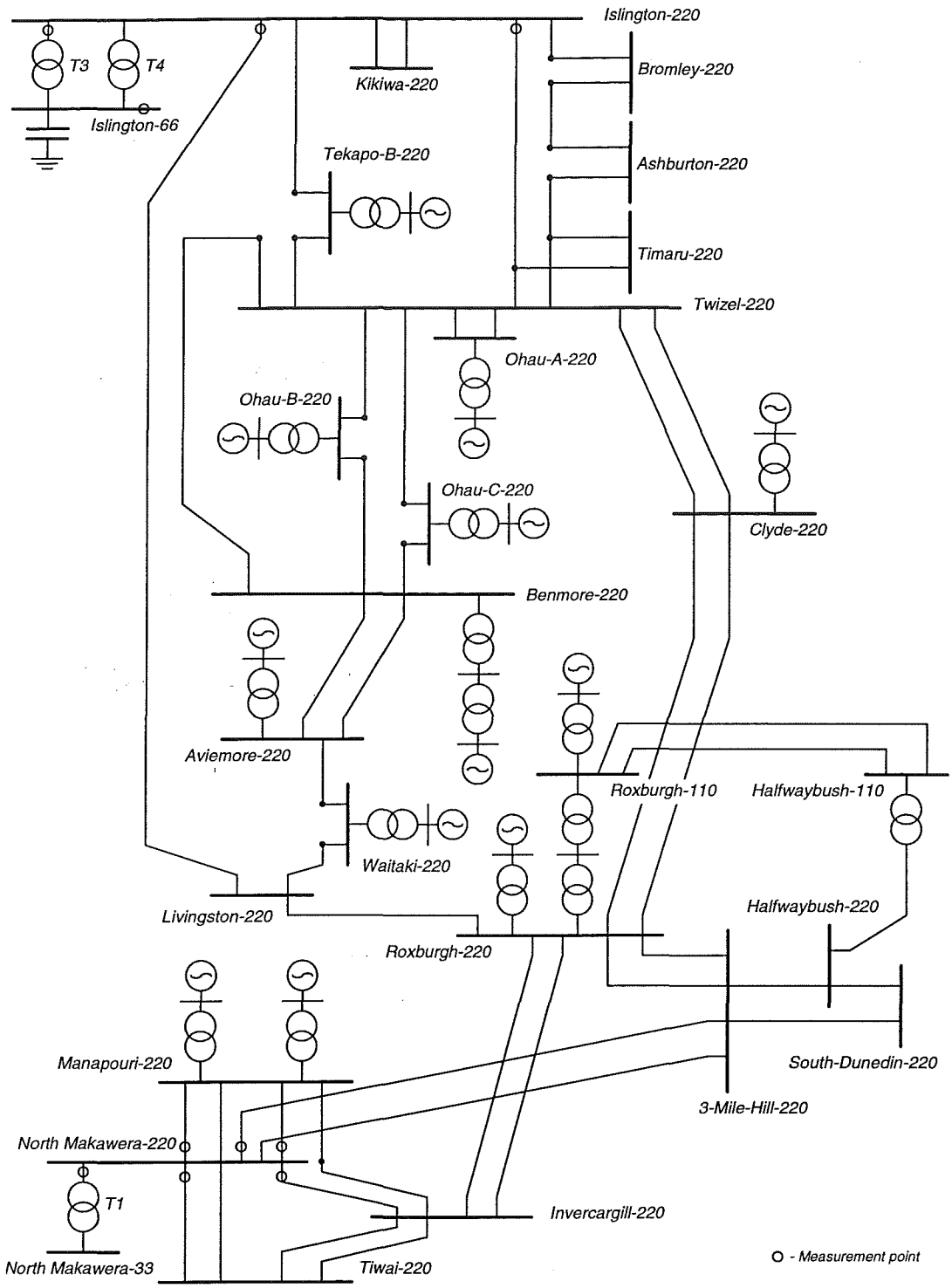

Figure 9-7: CHART measurement points in the Synchronised Test

At North Makawera, the main flow of power is between the generation at Manapouri and the aluminum smelter load at Tiwai. The CHART III unit was set up to monitor the current between these two places and the North Makawera substation. The connections from North Makawera to the rest of the 220kV network were also monitored by measuring the current between North Makawera and 3 Mile Hill, and between North Makawera and Invercargill. The current of transformer T1 feeding the 33kV distribution network at North Makawera was monitored to determine if there is any 5^{th} harmonic source within the local load. The voltage

distortion on the 33kV distribution busbar was also recorded. However, due to the limited number of channels available on this particular CHART III unit (12 channels), it was necessary to forgo some of the phases at several measurement points.

The main requirement of this test was to record the harmonic distortion at both substation simultaneously. The data samples are to be time-stamped to enable them to be matched in time. It was decided to average the harmonics over one second and to compute the mean, maximum and minimum harmonics over a minute throughout the entire measurement. These requirements call for special design of the DSM and DAPM applications in the CHART III system.

Figure 9-8 shows the operation of the DSM in this test. The Sample Rate Multiplier (SRM) of the DSM is initialised to generate 1024 sampling pulses per fundamental cycle. The mains frequency at both substations are used as the reference for the fundamental frequency. The sampling pulses are gated at the P2 Interface and the DSM application decides when the pulses are to be dispatched onto the P2 time-stamping bus. The DSM application monitors the precision 1 pps (pulse per second) and the date and time information received from the GPS system. Through the parameter setup process of the CHART III virtual operating system, the DSM application is programmed to release the sampling pulses at a user-configurable time. The application can also be configured with a pre-defined stop sampling time. Upon the arrival of every 1 pps, which is also used to register the new date and time received from the GPS system, the DSM application compares the new time against the pre-defined start-sampling and stop-sampling time. If the new time falls between them, the gate in the P2 interface is opened, releasing the sampling pulses onto the P2 bus. This method of making use of the precision 1 pps to initiate and terminate the sampling process ensures that the data is acquired at the same instants in both substations.

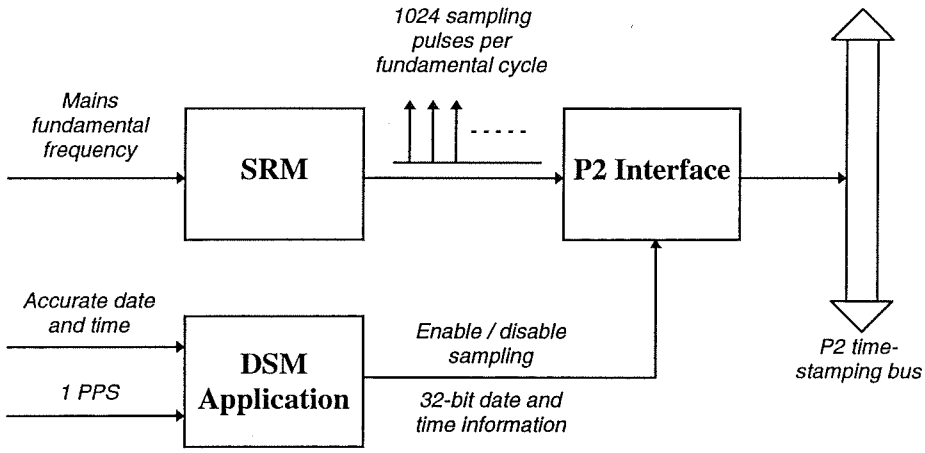

Figure 9-8: Operation of the DSM in the Synchronised Test

The DAPM application is programmed to operate on a cycle-by-cycle basis with 1024 samples designated as one cycle. Figure 9-9 shows the data processing carried out by the DAPM application in the synchronised test. This application operates over every 3000 cycles corresponding to one minute if the fundamental frequency remains constant at 50 Hz.

The 1024 samples per cycle of raw time domain data is passed through a FIR filter with 8:1 decimation to reduce the number of samples to 128. Every ten filtered cycles are averaged to form and the harmonic information is obtained by applying the FFT to the averaged cycle. This process results in 300 sets of harmonic packets and every five of them are again

averaged to produce one-second harmonic averages. The mean, maximum and minimum harmonics over a minute are then computed from the sixty packets of one-second averages. The five averaged time domain cycles used to compute the FFT are dispatched from the DAPM application alongside the one-second harmonic averages. This provides the option of analysing the time domain waveform if there are doubts about the computed harmonic information. The HUB processor of the CHART system was set up to store these five forms of data over the entire test.

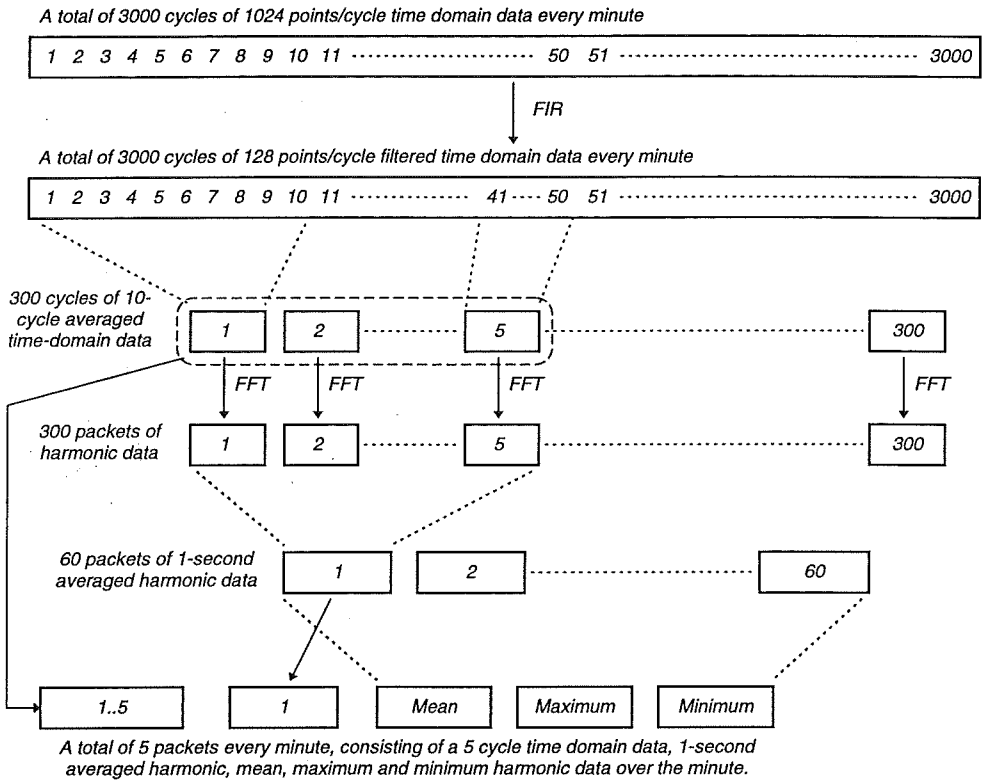

Figure 9-9: Data processing carried out by the DAPM in the Synchronised Test

9.7 Summary of the Synchronised Test

The test was carried out over a period of thirteen hours with the two CHART III units initiated simultaneously through the synchronisation mechanism built into the DSM application. The measurement period was chosen to coincide with the switching-out of the capacitors at Islington substation which takes place during light load conditions. The test was started at 6:00pm on the 16th of November and finished on the next day at 7:00am. Although the one-second harmonic averages were computed every second, it was decided that the mean, maximum and minimum harmonics over a minute were sufficient and hence, the one-second averages and the corresponding five-cycle averaged waveform are only recorded once every minute.

The sampling process is initiated by the 1 pps received from the GPS system. During the course of the measurement, the DSM locks the sampling pulses to the system mains frequency. Therefore, if the mains frequency at both sites remain fairly similar to each other, the sampling processes in both CHART III units are synchronised. The measured fundamental frequencies at Islington and North Makawera are shown in Figure 9-10. The fundamental

frequencies are identical at both sites with similar deviations throughout the measurements. This has ensured that the sampling processes were synchronised between the two CHART III units.

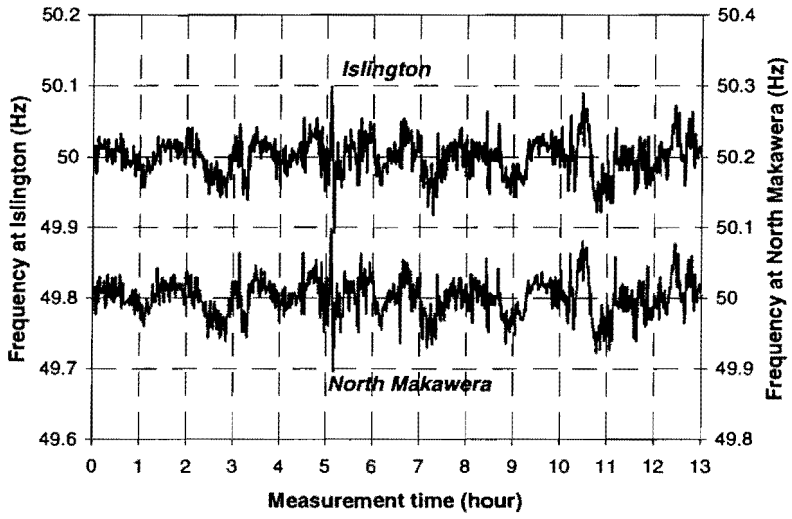

Figure 9-10: Fundamental frequency measured at Islington and North Makawera

A selection of acquired data is shown in Figure 9-11. A number of steps are observed on the 66kV bus voltage which may be caused by the switching of the compensation capacitors. However, only three of these show concurrent changes in the 5th harmonic current flowing out of the Islington substation. The three cases are highlighted in the figure together with the possible capacitor switching instants. The currents in the two transmission lines, Islington-Livingston and Islington-Timaru-Twizel, show an increase in the 5th harmonic current when the capacitors are switched out. A decrease in the 5th harmonic current is also observed when the capacitor is switched back into service towards the end of the test.

The variations in the 5th harmonic current at North Makawera do not always correspond with the changes at Islington. Among the three aforementioned instants when there are changes to the 5th harmonic current flowing out of Islington, only the last two show corresponding changes in the distortion at North Makawera. At the second highlighted switching just after the 7th hour, when one of the capacitors is removed from service, the sudden increase in the 5th harmonic currents in the two outgoing lines from Islington coincides with similar increases in the lines between 3-Mile Hill, North Makawera and Tiwai. Similar coincidence is observed when one of the capacitors is put back into service near the end of the test. The decrease in the 5th harmonic current flowing out from Islington 220kV system coincides with the decreases in the 5th harmonic distortion around North Makawera. These observations indicate that under certain operating conditions, the switching of capacitors at Islington substation can affect the 5th harmonic distortions at North Makawera. More detailed analyses of the system, in particular during the period when the measurement was carried out, will be required to finalise the above findings. A more comprehensive analyses of the acquired data will be undertaken by Trans Power to work out the configuration of the system that enhances such a connection between the 5th harmonic problems at the two substations.

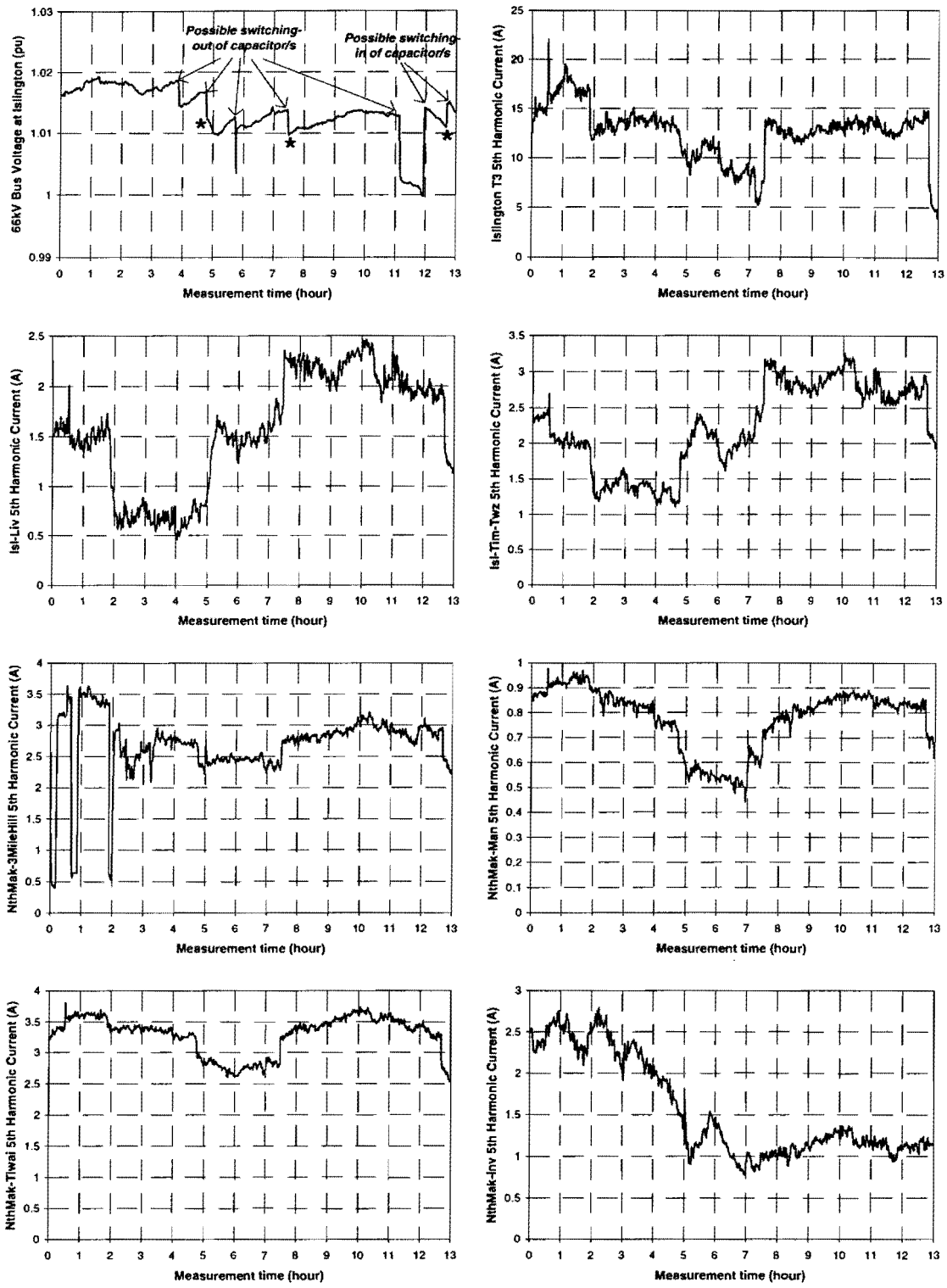

Figure 9-11: Selection of data acquired in the South Island Synchronised Test

9.8 Conclusion

These two field measurements have examined the flexibility provided by the CHART III system. The modular nature of the system has enabled different data processing algorithms to

be programmed into the system with ease. The implementation of the CHART III Virtual Operating System has streamlined the setting up of the processing algorithm and the transparent handling and storing of the captured data. The flexibility built into the CHART III system has made it possible to undertake these two tests within one week. Although the acquired data has not yet been fully analysed, preliminary studies have indicated the success of the CHART III system in capturing the desired information and in fulfilling the objectives of the tests.

Chapter 10

Conclusions And Future Work

10.1 Conclusions

A linearised frequency domain model of the HVDC convertor transformer core saturation instability has been described. A term, referred to as the *Saturation Stability Factor*, initially proposed by [Wood, 1993] for assessing the system susceptibility to this type of instability, has been extended to consider more realistic transformer properties. This instability has been classified into two categories depending on their starting conditions; the kick-started and the spontaneous instability. The *Saturation Stability Factor* has been shown to be accurate in the prediction of both kinds of instability, and sufficient agreement was observed between the predictions and the time domain simulations to instill confidence in this simplified model.

The quick solution and low computation burden of the technique provides a convenient way to generate an overview of the phenomenon. It has been used to reveal the characteristics of HVDC systems prone to this type of instability. A susceptible rectifier system was discovered to possess the following characteristics:

- A low and predominantly capacitive dc side impedance at the fundamental frequency, with the presence of a series resonance at a frequency slightly higher than the fundamental frequency.
- A high and predominantly inductive ac side second harmonic impedance, with the presence of a parallel resonance at a frequency just above the second harmonic.
- A relatively high resistance on the ac side near 0Hz.

On the other hand, a vulnerable invertor system exhibits a fairly similar characteristic to the rectifier system, except that the resonance frequencies are lower than the fundamental frequency on the dc side, and lower than the second harmonic on the ac side respectively. A high ac side resistance near 0Hz still enhances the instability at the invertor end.

Besides the system impedance characteristics, the likelihood of developing the instability corresponds closely to the convertor transformer susceptibility to core saturation. Transformers with low knee points are easily saturated by relatively low dc current, while those with low saturated reactances cause large distortion when they are saturated. Both of these effects can combine to degrade the system stability.

The steady state operation parameters of the convertor have been shown to affect the system stability. Increasing the firing angle at the rectifier (or reducing the firing angle at the invertor) reduces the *Saturation Stability Factor*, not only by its own accord, but the consequential shortening of the commutation process has reduced the damping on the system. Fortunately, the HVDC scheme is usually operated with low firing angle at the rectifier (and

low extinction angle at the invertor) to minimise the reactive power requirement, and this common practice has helped to minimise the risk of developing such an instability.

The convertor controller has been shown to exercise a strong influence on the system stability. In particular, the development of the core saturation instability always involves a destabilising contribution from the convertor controller. Consequently, this can be prevented through alterations of the controller parameters, or by introducing an auxiliary control around the main controller. Moreover, the influence of the controller was shown to vary significantly with the changes in the system. This complicates the selection of control measures as the controller responses under all possible operating conditions have to be considered. However, the ability of the *Saturation Stability Factor* to quickly indicate the relative stability of one system from another has made it easier to determine the unstable areas and to achieve appropriate control solutions.

In the back-to-back scheme, the stability of one convertor station is affected by the opposite end convertor and the characteristics of the connected ac network. Due to the opposite requirements of the system impedances for the instability to occur at the rectifier and the invertor, the instability is expected to occur only at one end of a back-to-back scheme. However, the strong influence of the convertor controllers may alter the effects of the impedances such that the instability develops at both ends. This highlights the need to consider the response at both ends when designing control measures for back-to-back schemes.

The direct indication of the system stability by the *Saturation Stability Factor* has eliminated the need for trial and error approach in the search for control solutions. The most effective solutions can be easily determined by comparing the *Saturation Stability Factor* for different control configurations. Several possible control measures are illustrated in the thesis with the controller parameters determined from the evaluation of the *Saturation Stability Factor.* These demonstrations have proven the *Saturation Stability Factor* approach as an effective design tool. However, it is important to remember that it only shows the system strength against core saturation instability. Therefore, it is necessary to verify that any control measure based on the evaluation of *Saturation Stability Factor* does not enhance the development of other types of instability.

Although off-line PSCAD/EMTDC computer simulations illustrated successfully the build up of core saturation instability in the time domain, the long simulation time makes it a rather elaborate and time consuming process. Real time simulators such as the RTDS or a scaled-down hardware model would be ideal for studying this type of phenomenon. These alternatives will shorten the simulation time and assess the performance of the detection and control techniques in a somewhat more realistic operating environment. However, a real time simulator requires a companion data acquisition system to process and present the simulated data. New detection and control techniques need to be tested on an on-going basis and hence, the data acquisition system must be capable of taking up new processing algorithms as well as new displays for the presentation of data of varying formats.

The requirements of such a flexible data acquisition system have been outlined in Chapter 6. Among them, the continuous data processing in real time is considered mandatory, in order to avoid the loss of any event which may happen if only snap shots are taken. Moreover, the ability to accurately time-tag the acquired samples simultaneously is vital for post-processing the acquired data. Despite the remarkable advances in the electronic industry, no existing data acquisition system is able to meet all these requirements. A locally developed system called CHART has been shown to possess the potential to fulfill these requirements. However, its

previous versions, CHART I and CHART II, were oriented solely at harmonic measurements, even though the modular structure has the capacity to perform other functions.

The retirement of a key proprietary processing board used in CHART II had brought about the development of CHART III. The new system has a generally similar structure to its predecessor, but is constructed with more industrial standard hardware and software. The philosophy of using industrial standard components, hardware and software, has ensured continued future expansion and upgrade opportunities, and has improved the compatibility of the system with other commercial tools. In line with the development of CHART III, a new software architecture has been designed to extend the capability of the CHART system beyond harmonic measurements.

The new software architecture is referred to as the CHART III Virtual Operating System due to its resemblance to a typical computer operating system. The design is based on the philosophy that a flexible data acquisition tool should allow customised processing algorithms to be implemented at the front ends near the source of the data, while at the same time enable the use of specialised setup, control and display interfaces at the user end. To enable the implementation of customised algorithms, the software is divided into two parts; an operating layer or system, and a user-definable application. The operating layer or system serves the application, providing it with the core functionalities to decide how the data samples are acquired and processed, and to dispatch the processed data from the front end to the user interface. The user decides on the data processing algorithm through the definition of the application. There is also the provision for user to design customised setup, control and display user interfaces, while making use of the transparent interfaces provided by the virtual operating system to issue control and setup commands to the processors and to receive the processed data. The system also facilitates the storage and retrieval of the stored data for further analysis.

The CHART III Virtual Operating System is implemented with industrial standard software, maximising its compatibility with other commercial presentation and analysis tools. This has streamlined the process of analysing the acquired data, and assisted in the generation of reports. Moreover, the modular architecture has greatly reduced the complications commonly encountered in the upgrade and expansion processes. The virtual operating system has decoupled one hardware item from another, enabling gradual expansion of the system in manageable stages.

The flexibility provided by CHART III has been demonstrated with two field measurements, each possessing widely differing data processing requirements. With the core functionalities provided by the virtual operating system, the task of preparing for these measurements has been simplified to the definition of the specialised data processing algorithms. The flexibility built into the CHART III system has made it possible to really carry out both measurements soon after each other.

Even though the CHART III system has not been used to analyse the convertor transformer core saturation instability as originally planned, the capability of CHART III proven by the two field tests, and the appreciation of the instability problem gained through the linearised analysis, have paved the way for real time studies of this phenomenon as soon as the availability of a real time simulator or a scaled-down model is resolved.

10.2 Future work

10.2.1 Convertor transformer core saturation instability

The continued analysis of the convertor transformer core saturation instability can be approached from two distinct directions; a theoretical viewpoint or a practical viewpoint in consideration of utilising CHART III. The former involves the continued refinement of the *Saturation Stability Factor* for analysis of specific convertor configurations. The existing derivation considers the stability of a single 12-pulse convertor pole, but most of the existing schemes comprise two poles, customarily in series to achieve a bipolar configuration. Although most of the bipolar schemes have similar construction at both poles, they are sometimes controlled separately, complicating the assessment of the overall stability of the scheme. The different convertor configurations used in positive and negative poles, such as in the upgraded New Zealand scheme, have further complicated the analysis. New convertor models can be defined to take into account any of the specific convertor configurations.

Still in line with the improvement of *Saturation Stability Factor*, the model so far has considered the stability at only one end of the link. This is applicable for long distance dc transmission schemes, but is clearly inadequate for back-to-back intertie. This approach can be extended to consider the overall stability of both convertor systems in tandem, with consideration of the destabilising contributions from the convertor transformers at both ends of the link.

The second direction of future work reflects the real time analysis of the core saturation instability. This not only provides the opportunity to further verify the capability of the CHART III system, but would also enable the proposed control measures to be assessed in a pseudo real operating power system. The practical issues concerning the implementation of the control solutions can also be resolved.

Most of the illustrations in the thesis relate to the kick-started version of the instability. This was chosen due to the shorter simulation time compared to its spontaneous counterpart. The availability of a real time simulator will greatly alleviate this problem and allow more analysis to be undertaken on this category of core saturation instability. The CHART III system, with its continuous data processing capability is ideal for detecting the slow development of spontaneous instability, but the detection technique has yet to be developed. Furthermore, the control solutions for the spontaneous instability may be different from the kick-started version, since a less drastic action is required if early detection is available.

If there are difficulty over the availability of a real time digital simulator, a scaled-down hardware model can be constructed for such studies. Accurate models of the major components around the convertor will be needed, and the experimental system may need to be excited to induce the development of the instability. The additional damping customarily found in scaled-down hardware models need to be carefully considered. This line of studies will provide another opportunity to verify the *Saturation Stability Factor* technique, and should contribute to refining the approach.

Irrespective of the aforementioned directions, more analysis on the possible control measures is required. The studies described in this thesis have yet to quantify the various control solutions. More thorough examination of each of the control techniques, taking into account the impact of the controller on other requirements of the system, is required to rank the effectiveness and suitability of each control solution. Since the vast majority of the measured

signals and the control signals are digitised, it would be appropriate to implement the controller by digital methods. One possibility is the use of a digital FIR filter as an auxiliary controller, either in the band pass or high pass configuration. The need to tune the phase response of the filter may result in a considerable filter length, but the long time constant of the instability may have eliminated the need for fast response, facilitating such a lengthy filter arrangement.

The frequency specific nature of the mechanism implies that a narrow band controller may be sufficient to counter the instability, while at the same time not affecting the normal operation of the scheme. A controller based on a phase locked loop tuned to a particular frequency may prove to be a highly effective solution.

Last but not least, it would be excellent if the *Saturation Stability Factor* technique could be used to study the instability problem in an existing scheme. This will put the accuracy of the simplified technique as well as the past techniques used to solve the problem, in close scrutiny.

10.2.2 CHART

The upgrade and expansion opportunities of the CHART III system have been described in Chapter 7. The modular structure has removed the constraints on future expansions, customarily found in existing data acquisition systems. The use of standard hardware and software has ensured smooth future upgrades to more powerful processors, and more effective and reliable software. Although the system has the provision for unlimited scope in new hardware and software, it is probably better to concentrate on exploiting the capability of the existing system. The two tests described in the thesis have merely scratched the surface of its capacity. New applications not only help to iron out the errors in the current system, but their requirements will pinpoint the development direction and serve to prioritise the work to be undertaken on the system. Moreover, the use of CHART III is not confined to just power system analysis, and the opportunity exists to apply it in other areas.

The first new application would be the analysis of core saturation instability as soon as a digital real time simulator or a scaled-down model is available. This will call for a new suite of data acquisition software, determining how the data samples are taken, processed and presented. New interfacing hardware may be required if the current version (Type A RDCM) is inadequate. Moreover, the use of the system as a controller needs to be explored. To detect the development of the core saturation instability, particularly the spontaneous type, the system needs to maintain a constant vigil, ideally suited to the continuous monitoring capability of CHART III. The current system has been designed with limited provision to initiate control actions. Both hardware and software extension are needed to achieve a user-definable controller.

With the experience from the two field measurements, the obvious improvement in the system is a new three-channel Remote Data Conversion Module (RDCM). It is usual to find that the measuring points of the three phases of voltage or current are situated physically close to each other. A three-channel unit would greatly reduce the bulk of the system, effectively by a factor of three. However, the added computational burden on a single processor has to be carefully weighed against the convenience of smaller size equipment. It may be necessary or even wise to include a processor within the three-channel unit to increase the system processing capacity. Lastly, the three-channel unit would be a useful addition for the analysis

of core saturation instability, as it is necessary to compute the sequence components for both detection and control measures.

Secondly, the existing Type A RDCM has been designed to operate up to a sampling rate of tens of kHz. This is adequate for most of the studies, particular those in steady state, but is inadequate for capturing fast transient waveforms. A fast response unit with a high sampling rate and a wide dynamic range will be needed for fault or transient analysis. A considerable amount of memory may have to be provided in the unit for buffering the samples before carrying out any processing or dispatching them to the rest of the system.

Apart from the new versions of hardware, new software will emerge with new applications. New control, setup and display user interfaces will be designed alongside new data processing algorithms. Extension of the virtual operating system or layer may be required to pass on the flexibility built in the existing system to the new components.

The software architecture in the PPU is based on a many-to-one arrangement, with multiple processors dispatching data to a central collecting point at the HUB. This design is inherited from the data acquisition role of the system, and needs to be revised to extend its role to carry out control actions. A many-to-many orientation of the communication between the processors in the system may be sufficient to fulfill this responsibility. This layout would enable additional processing boards to be incorporated into the PPU, receiving data from the other processors and issuing specific control signals either directly to the real time simulator, or through some mediator control circuitry.

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Appendix A

The convertor frequency dependent equivalent

This appendix lists the equation sets used in [Wood, 1993] to define the harmonic impedance of the HVDC convertor. The description here is based on chapter 5 and appendix D of [Wood, 1993].

A.1 Convertor harmonic impedance

Considering only the most significant harmonics as outlined in Chapter 3, the relationships between the three harmonics around the HVDC convertor can be described with a set of simultaneous equations.

$$
\begin{aligned}
V_{dch} &= a_1 N\left(V_{acp} - a_5 Z_{xp} N I_{dch}\right) + a_2 N\left(V_{acn} - a_8 Z_{xn} N I_{dch}\right) + a_3 f_{am} + a_4 f_{ame} \\
I_{acp} &= a_5 N I_{dch} + a_6 N f_{am} + a_7 N f_{amd} \\
I_{acn} &= a_8 N I_{dch} + a_9 N f_{am} + a_{10} N f_{amd} \\
f_{ame} &= a_{11} N V_{acp} + a_{12} N V_{acn} + a_{13} I_{dch} + a_{14} f_{am} \\
f_{amd} &= a_{15} N V_{acp} + a_{16} N V_{acn} + a_{17} I_{dch} + a_{18} f_{am} \\
f_{am} &= a_{19} N V_{acp} + a_{20} N V_{acn} + a_{21} I_{dch} \\
V_{acp} &= -I_{acp} Z_{acp} + V_{acp0} \\
V_{acn} &= -I_{acn} Z_{acn} + V_{acn0} \\
I_{dch} &= V_{dch} / Z_{dch} + I_{dch0}
\end{aligned}
\qquad \textbf{(A.1)}
$$

where V_{acp} and I_{acp} are the positive sequence frequencies on the ac side at one harmonic higher than V_{dch} and I_{dch} on the dc side which is in turn at one harmonic higher than the negative sequence V_{acn} and I_{acn} on the ac side. Z_{xp} and Z_{xn} are the transformer leakage reactance at the two frequencies of positive and negative sequences respectively and are referred to the transformer line or primary side. f_{am} describes the modulation on the firing angle while f_{amd} and f_{ame} allows the variations in commutation period duration and the end of the commutation period to be represented in the system. N is the convertor transformer turn ratio referred to the primary side. Letting k be the frequency on the dc side of a 12 pulse convertor, the terms a_1 to a_{18} are calculated from the convertor steady state average operating parameters.

$$a_1 = \frac{6\sqrt{3}}{\pi}\cos\left(\frac{\mu_0}{2}\right)\angle\alpha_0 + \frac{\mu_0}{2}$$

$$a_2 = \frac{6\sqrt{3}}{\pi}\cos\left(\frac{\mu_0}{2}\right)\angle -\alpha_0 - \frac{\mu_0}{2}$$

$$a_3 = -\frac{NV_1 3\sqrt{3}}{\pi}\sin(\alpha_0)$$

$$a_4 = -\frac{NV_1 3\sqrt{3}}{\pi}\sin(\alpha_0 + \mu_0)\angle -k\mu_0$$

$$a_5 = \frac{2\sqrt{3}}{\pi}\frac{\sin\left(\frac{\mu_0}{2}\right)}{\frac{\mu_0}{2}}\angle -\alpha_0 - \frac{\mu_0}{2}$$

$$a_6 = I_d\frac{2\sqrt{3}}{\pi}\frac{\sin\left(\frac{(k+1)\mu_1}{2}\right)}{\frac{(k+1)\mu_1}{2}}\angle -\alpha_0 - \frac{(k+1)\mu_1}{2} - \frac{\pi}{2}$$

$$a_7 = I_d\frac{\sqrt{3}}{\pi}\left(\frac{\sin\left(\frac{\mu_1}{4}\right)}{\frac{\mu_1}{4}}\right)^2\angle -\alpha_0 - \frac{(k+1)\mu_1}{\sqrt{x}} - \frac{\pi}{2}$$

$$a_8 = \frac{2\sqrt{3}}{\pi}\frac{\sin\left(\frac{\mu_0}{2}\right)}{\frac{\mu_0}{2}}\angle\alpha_0 + \frac{\mu_0}{2}$$

$$a_9 = I_d\frac{2\sqrt{3}}{\pi}\frac{\sin\left(\frac{(k-1)\mu_1}{2}\right)}{\frac{(k-1)\mu_1}{2}}\angle\alpha_0 - \frac{(k-1)\mu_1}{2} + \frac{\pi}{2}$$

$$a_{10} = I_d\frac{\sqrt{3}}{\pi}\left(\frac{\sin\left(\frac{\mu_1}{4}\right)}{\frac{\mu_1}{4}}\right)^2\angle\alpha_0 - \frac{(k-1)\mu_1}{\sqrt{x}} + \frac{\pi}{2}$$

$$a_{11} = \left\{\frac{-\mu_0}{NV_1\sqrt{1-\left[\cos(\alpha_0) - \frac{2X_c I_d}{\sqrt{3}NV_1}\right]^2}}\right\}\cdot\frac{\sin\left(\frac{(k+1)\mu_0}{2}\right)}{\frac{(k+1)\mu_0}{2}}\angle\alpha_0 + \frac{(k+1)\mu_0}{2} - \frac{\pi}{2} \qquad \textbf{(A.2)}$$

$$a_{12} = \left\{ \frac{-\mu_0}{NV_1\sqrt{1-\left[\cos(\alpha_0)-\frac{2X_cI_d}{\sqrt{3}NV_1}\right]^2}} \right\} \cdot \frac{\sin\left(\frac{(k-1)\mu_0}{2}\right)}{\frac{(k-1)\mu_0}{2}} \angle -\alpha_0 + \frac{(k-1)\mu_0}{2} + \frac{\pi}{2}$$

$$a_{13} = \frac{2X_c\cos\left(\frac{k\mu_0}{2}\right)}{\sqrt{3}NV_1\sqrt{1-\left[\cos(\alpha_0)-\frac{2X_cI_d}{\sqrt{3}NV_1}\right]^2}} \angle \frac{k\mu_0}{2}$$

$$a_{14} = \frac{\sin(\alpha_0)}{\sqrt{1-\left[\cos(\alpha_0)-\frac{2X_cI_d}{\sqrt{3}NV_1}\right]^2}}$$

$$a_{15} = \left\{ \frac{3NV_1\mu_0}{2(X_cI_d)^2}\left[\sin(\alpha_0+\mu_0)-\sin(\alpha_0)-\mu_0\cos(\alpha_0)\right] \cdot \frac{\sin\left(\frac{(k+1)\mu_0}{2}\right)}{\frac{(k+1)\mu_0}{2}} \right\} \angle \alpha_0 + \frac{(k+1)\mu_0}{2} - \frac{\pi}{2}$$

$$a_{16} = \left\{ \frac{3NV_1\mu_0}{2(X_cI_d)^2}\left[\sin(\alpha_0+\mu_0)-\sin(\alpha_0)-\mu_0\cos(\alpha_0)\right] \cdot \frac{\sin\left(\frac{(k-1)\mu_0}{2}\right)}{\frac{(k-1)\mu_0}{2}} \right\} \angle -\alpha_0 + \frac{(k-1)\mu_0}{2} + \frac{\pi}{2}$$

$$a_{17} = \frac{\mu_0}{I_d}\left\{1+\left[\frac{\sin\left(\frac{k\mu_0}{2}\right)}{\frac{k\mu_0}{2}} \angle \frac{k\mu_0}{2}\right]\right\} + \frac{2}{kI_d}\left\{\left[\frac{\sin\left(\frac{k\mu_1}{2}\right)}{\frac{k\mu_1}{2}} \angle \frac{k\mu_1}{2}\right] - 1\right\} \angle \frac{\pi}{2}$$

$$a_{18} = \frac{\sqrt{3}NV_1}{X_cI_d}\mu_0\sin(\alpha_0) - 2$$

These terms depend on the average actual and effective commutation period defined as follows

$$\begin{aligned} \mu_0 &= \cos^{-1}\left[\cos(\alpha_0)-\frac{2X_cI_d}{\sqrt{3}NV_1}\right]-\alpha_0 \\ \mu_1 &= 2\mu_0 - \frac{\sqrt{3}NV_1}{X_cI_d}\left[\mu_0\cos(\alpha_0)+\sin(\alpha_0)-\sin(\alpha_0+\mu_0)\right] \end{aligned} \qquad \textbf{(A.3)}$$

where V_1 is the peak single phase ac voltage at the convertor transformer primary, X_c is the convertor transformer leakage reactance referred to the transformer secondary and I_d is the steady state dc current.

Terms a_{19}, a_{20} and a_{21} depend on the transfer function of the convertor controller. For proportional and integral type of constant current controller,

$$\begin{aligned} a_{19} &= 0 \\ a_{20} &= 0 \\ a_{21} &= PG + \frac{1}{j\omega TI} \end{aligned} \tag{A.4}$$

where PG is the proportional gain and TI is the integral time constant.

The interrelationship between the three harmonic sequences around the 12 pulse HVDC convertor expressed as simultaneous equation set of A.1 can be reduced and rewritten as a three-by-three matrix as follow

$$\begin{bmatrix} V_{dch} \\ I_{acp} \\ I_{acn} \end{bmatrix} = \begin{bmatrix} a & b & c \\ d & e & f \\ g & h & i \end{bmatrix} \cdot \begin{bmatrix} V_{acp} \\ V_{acn} \\ I_{dch} \end{bmatrix} \tag{A.5}$$

with the following assignments,

$$\begin{aligned} a &= a_1 N + a_3 a_{19} N + a_4 a_{11} N + a_4 a_{14} a_{19} N \\ b &= a_2 N + a_3 a_{20} N + a_4 a_{12} N + a_4 a_{14} a_{20} N \\ c &= -a_1 a_5 N^2 Z_{xp} - a_2 a_8 N^2 Z_{xn} + a_3 a_{21} + a_4 a_{13} + a_4 a_{14} a_{21} \\ d &= a_6 a_{19} N^2 + a_7 a_{15} N^2 + a_7 a_{18} a_{19} N^2 \\ e &= a_6 a_{20} N^2 + a_7 a_{16} N^2 + a_7 a_{18} a_{20} N^2 \\ f &= a_5 N + a_6 a_{21} N + a_7 a_{17} N + a_7 a_{18} a_{21} N \\ g &= a_9 a_{19} N^2 + a_{10} a_{15} N^2 + a_{10} a_{18} a_{19} N^2 \\ h &= a_9 a_{20} N^2 + a_{10} a_{16} N^2 + a_{10} a_{18} a_{20} N^2 \\ i &= a_8 N + a_9 a_{21} N + a_{10} a_{17} N + a_{10} a_{18} a_{21} N \end{aligned} \tag{A.6}$$

A.2 Convertor equivalent dc side impedance

In the study of convertor transformer core saturation instability, the remote end convertor and the impedances of the remote end ac system have to be combined and represented as an equivalent dc impedance. With further assignments made from the above reduced equation set A.6, the impedance of the convertor including the ac side impedances looking from the convertor dc terminal can be written as

$$Z_{convdc} = -\left(\frac{AD}{1-C} + B\right) \tag{A.7}$$

and with the following assignments.

$$A = -aZ_{acp} + \frac{bgZ_{acn}Z_{acp}}{1+hZ_{acn}}$$

$$B = c - \frac{biZ_{acn}}{1+hZ_{acn}}$$

$$C = \frac{egZ_{acn}Z_{acp}}{\left(1+dZ_{acp}\right)\left(1+dZ_{acn}\right)} \qquad \textbf{(A.8)}$$

$$D = \frac{f}{1+dZ_{acp}} - \frac{eiZ_{acn}}{\left(1+dZ_{acp}\right)\left(1+hZ_{acn}\right)}$$

Appendix B

Description of the HVDC Test Systems

B.1 Introduction

This appendix describes the HVDC test systems used in the thesis to illustrate the mechanism of the core saturation instability. These systems are modified from the 60 Hz version used by Burton in his study of the core saturation instability [Burton, 1994]. The prime objective of using these simplified fictitious test systems is to better the understanding of the mechanism of the instability and to illustrate its complex properties. These test systems are also used in the dynamic simulations for the verification of the direct frequency domain approach used in this research.

B.2 Test system without considering convertor controller

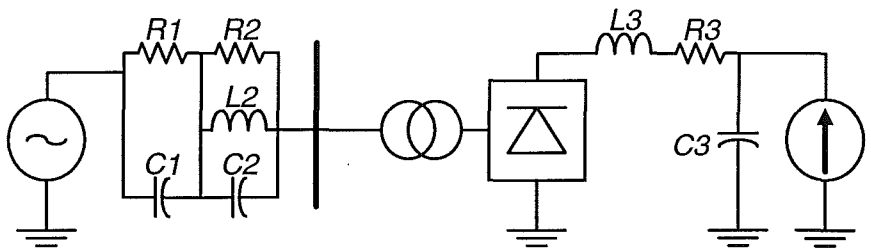


Figure B-1: Schematic diagram of the test system without convertor controller

Figure B-1 shows the schematic diagram of the fictitious HVDC test system used in the thesis when the effect of the convertor controller is ignored. It consists of a 12-pulse rectifier with the ac and dc systems simplified to equivalent RLC circuits. Without the convertor controller, the firing angle is locked to a constant value while the dc current is fixed by the current source which represents the invertor. This system is unique such that individual harmonic impedances related to the core saturation instability can be varied without adversely affecting the impedances at other frequencies. The resistor $R1$ is used to determine the ac side resistance at 0 Hz. The capacitor $C1$ connected in parallel to $R1$ has been intentionally made large so that it bypasses the effect of changing $R1$ on the ac side impedance at higher frequencies.

On the other hand, the $R2$, $L2$ and $C2$ components are used to define the ac side higher order harmonic impedances. They are used in this study to determine the characteristics of the ac side second harmonic impedance which affects the development of the instability. They are also used to tune a parallel resonance near the second harmonic frequency. On the dc side, the $R3$, $L3$ and $C3$ components form a path for the distorting harmonic currents. They are utilised

to define the dc side fundamental frequency impedance which plays a vital part in the instability mechanism.

With this test system, the three aforementioned harmonic impedances concerning the mechanism of the instability can be individually varied and their individual effect on the system susceptibility can be separately analysed. Table B-1 shows the base case values of the various components used in the system and the instability related harmonic impedances. The details of the convertor transformers are summarised in Table B-2.

$R1$ (Ω)	100.0
$C1$ (μF)	1000.0
$R2$ (Ω)	1030.0
$L2$ (mH)	6.42
$C2$ (μF)	378.92
$R3$ (Ω)	0.0
$L3$ (mH)	600.0
$C3$ (μF)	11.03
AC side resistance at 0 Hz	100.0
AC side second harmonic admittance (mhos)	0.001 - j0.010
DC side fundamental frequency admittance (mhos)	0.0 + j0.010

Table B-1: Component values of the test system

Transformer MVA rating (MVA)	80.118
Transformer voltage ratio (kV rms. phase to phase)	100.0 / 41.0955
Transformer leakage reactance (pu)	0.13
Transformer air core reactance (pu)	0.20
Transformer saturation knee point (pu)	1.25
Transformer magnetising current (% of the rated current per winding)	2

Table B-2: Descriptions of the convertor transformer

B.3 Test system incorporating convertor controller

In order to include the function of rectifier controller, the dc side of the test system is modified as shown in Figure B-2. With constant current controller at the rectifier, the invertor is modelled as a constant voltage source. The value of this voltage source is tuned according to the required resultant firing angle at the rectifier. The new components of $R4$, $L4$ and $C4$ are chosen such that the resultant capacitance at the fundamental frequency is similar to that of $C3$. The values of these new components are presented in Table B-3.

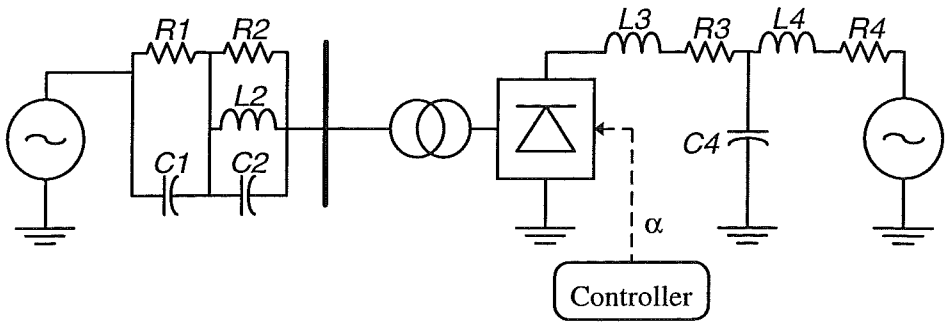


Figure B-2: Schematic diagram of the test system incorporating convertor controller

*R*4 (Ω)	1.0
*L*4 (mH)	918.0
*C*4 (μF)	22.07

Table B-3: Component values for the test system with convertor controller

B.4 Procedure used to kick-start the instability

The development of the convertor transformer core saturation instability has a very long time constant (in term of several minutes) and therefore will consume enormous amount of computation time. Therefore, Burton devised a time-scaling technique to artificially saturate the transformer through a constant modulation on the convertor firing angle order. In his study [Burton, 1994], a fundamental frequency modulation was introduced to the firing angle order, with the magnitude being ramped up to ±5° over 50 ms. This oscillation is then held constant for 350 ms and the modulation is ramped down over the next 100 ms. Therefore, half a second after the initial introduction of the modulation, the external driving disturbances are removed and the stability of the system is determined from the system response to the remaining distortions.

This procedure is adapted and modified to analyse the kick-started type of core saturation instability. Instead of using a constant ±5° modulation, the extent of this disturbance is determined from the intended level of saturation on the transformer. In this research, comparative systems are induced to similar level of transformer core saturation and the stability of the system is deduced from the system ability to settle itself back to the original pre-disturbance conditions.

Appendix C

Combined effect of system impedances on Saturation Stability Factor

C.1 Introduction

In Chapter 4, it was shown that the *SSF* of a HVDC system and its stability is characterised by the impedance profile of both its ac and dc systems. In order to highlight the effect of a single harmonic impedance, the other impedances were tuned to highly unstable values. In this appendix, these individual effects from the impedances are combined to evaluate whether these relationships with *SSF* will still hold if the other harmonic impedances are deviated from the unstable values. The harmonic impedances to be analysed are the ac side resistance at 0 Hz (R_{acn}), the ac side second harmonic impedance (Z_{acp}) and the dc side impedance at the fundamental frequency (Z_{dch}).

C.2 AC side resistance at 0 Hz

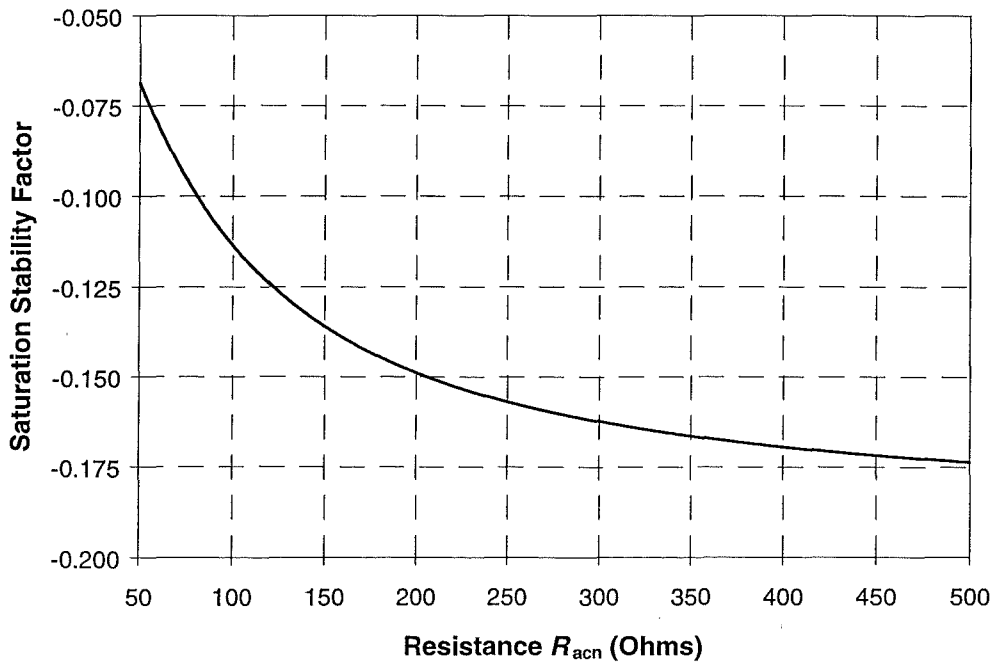


Figure C-1: *SSF* versus R_{acn} (base case)

The ac side resistance at 0 Hz (R_{acn}) was discovered to have an inverse relationship with the *SSF* as shown in Figure C-1. In this base case, both the ac side second harmonic admittance ($1/Z_{acp}$) and the dc side fundamental frequency admittance ($1/Z_{dch}$) were tuned to highly unstable values of 1.0 - j10.0 milli Siemens and 0.0 + j10.0 milli Siemens respectively. The relationship between R_{acn} and *SSF* is now reevaluated with different ac and dc side admittances. Figure C-2 shows the new *SSF* versus R_{acn} curves with less inductive Z_{acp} (i.e. susceptance being lowered to -j30.0 milli Siemens) and a capacitive Z_{acp} (i.e. susceptance changed to positive at +j10.0 milli Siemens). On the other hand, Figure C-3 shows the same relationship when Z_{dch} is altered to become inductive (i.e. susceptance of -j10.0 milli Siemens) or reducing its capacitance (i.e. susceptance raised to +j30.0 milli Siemens).

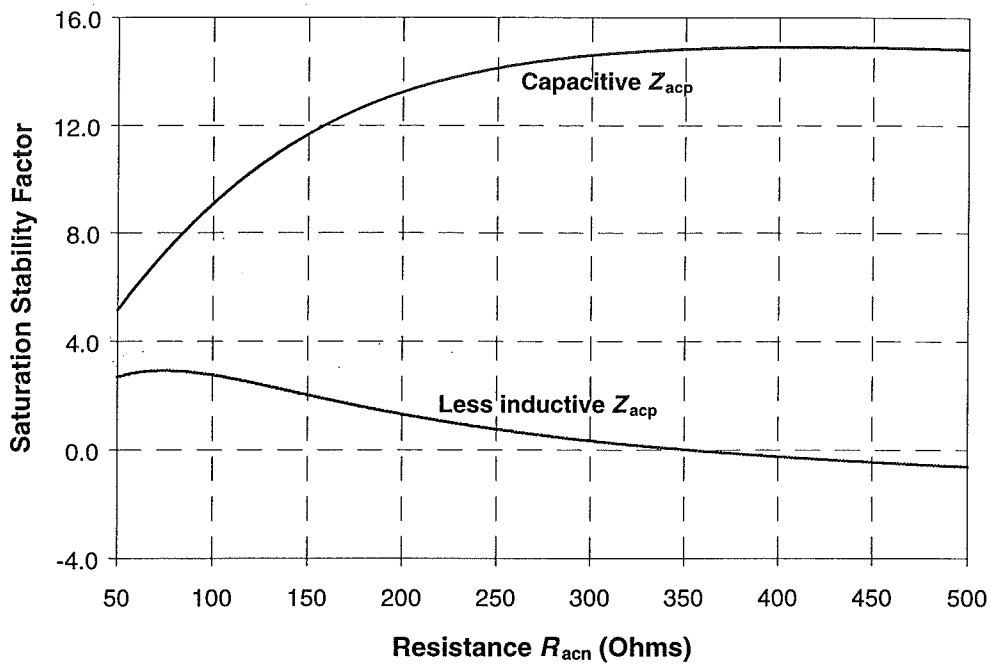


Figure C-2: *SSF* versus R_{acn} with different Z_{acp} characteristics

When Z_{acp} is made capacitive (i.e. $1/Z_{acp}$ = 1.0 + j10.0 milli Siemens), the *SSF* of the test system increases with R_{acn}. This behaviour contradicts the original relationship when the ac side impedance was inductive at the second harmonic frequency. Furthermore, the *SSF* remains positive throughout the range of R_{acn} considered, which indicates that the system remains stable irrespective of the value of R_{acn}. On the other hand, if the second harmonic impedance is made less inductive by lowering the susceptance to -j30.0 milli Siemens, the *SSF* is positive at low R_{acn} up to about 350.0 ohms and becomes becomes negative for higher R_{acn} depicting the vulnerability of the system to core saturation instability.

When the dc side impedance at the fundamental frequency Z_{dch} is made either inductive (i.e. $1/Z_{dch}$ = 0.0 - j10.0 milli Siemens) or less capacitive (i.e. $1/Z_{dch}$ = 0.0 + j30.0 milli Siemens), the relationship between *SSF* and R_{acn} reverses from that of the base case where Z_{dch} was more capacitive (i.e. $1/Z_{dch}$ = 0.0 +j10.0 milli Siemens). In both cases the *SSF* increases with R_{acn} and remains positive throughout the entire range of R_{acn}.

The above analysis has confirmed the dependency of the relationship between *SSF* and R_{acn} on the characteristics of the other two harmonic impedances Z_{acp} and Z_{dch}. Only when Z_{acp} is

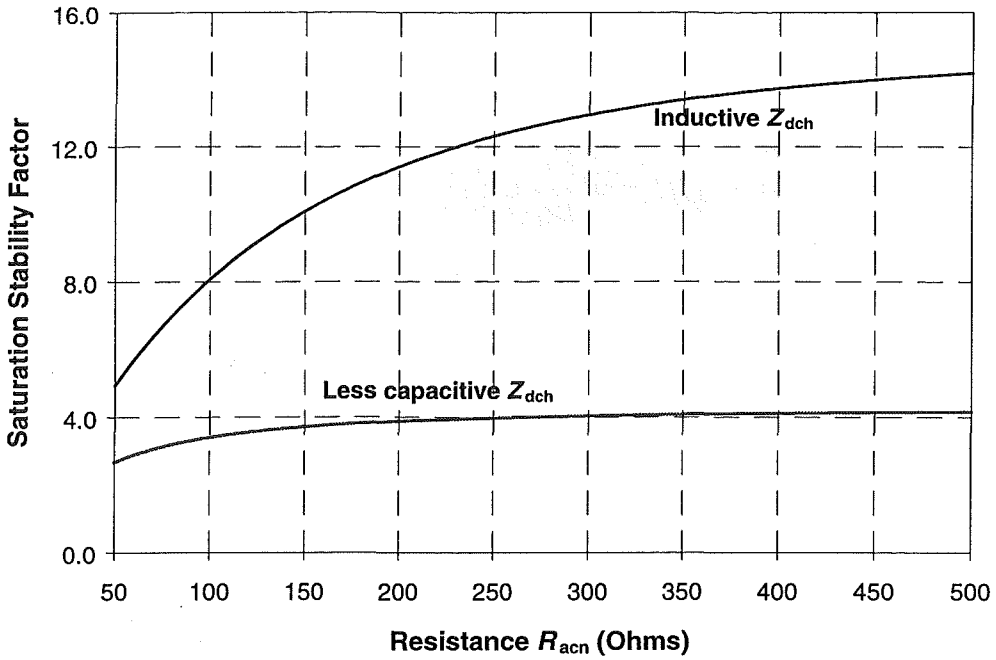


Figure C-3: *SSF* versus R_{acn} with different Z_{dch} characteristics

lightly inductive and Z_{dch} is capacitive, R_{acn} has a significant influence on the system susceptibility to core saturation instability. With other values of Z_{acp} and Z_{dch}, the system remains stable irrespective of the value of R_{acn}.

C.3 AC side second harmonic impedance

The appearance of core saturation instability in HVDC schemes was found to require an inductive second harmonic impedance on the ac side. This judgement was based on the assumption that the other two impedances R_{acn} and Z_{dch} are within their unstable ranges. For the base case used in Chapter 4, the ac side resistance R_{acn} and the dc side fundamental frequency admittance were fixed at 100 ohms and 0.0 + j10.0 milli Siemens respectively. The corresponding *SSF* and Z_{acp} relationship is shown in Figure C-4 and the range of admittance ($1/Z_{acp}$) with negative *SSF* is shown in Figure C-5. In this section, this relationship is examined with different values of R_{acn} and Z_{dch}.

Figure C-6 shows the new relationship between *SSF* and Z_{acp} when R_{acn} is changed from the base case value of 100 ohms to 10 and 200 ohms respectively. With lower R_{acn}, the *SSF* surface is levelled to a value around unity and with much smaller variation in *SSF* over the entire range of admittance. On the other hand, a higher R_{acn} increases the variation of *SSF* with Z_{acp}. This implies that the level of Z_{acp}'s influence on the *SSF* depends on the value of R_{acn}. Higher R_{acn} will see a greater influence from Z_{acp} to the *SSF* while low R_{acn} tends to mask the effect of Z_{acp}. However, the range of Z_{acp} where the *SSF* is negative is still confined to the area with low conductances and low and negative susceptances. Figure C-7 shows the unstable ranges of ac side second harmonic admittance for low and high R_{acn}. This observation shows that, even though changes in R_{acn} will alter the impact from Z_{acp} and also widen or narrow the unstable admittance regions, the second harmonic impedance Z_{acp} must still be low and inductive for the instability to develop. This implies that the presence of a

parallel resonance on the ac side at a frequency slightly higher the second harmonic is an essential condition for the development of the instability irrespective of the value of R_{acn}.

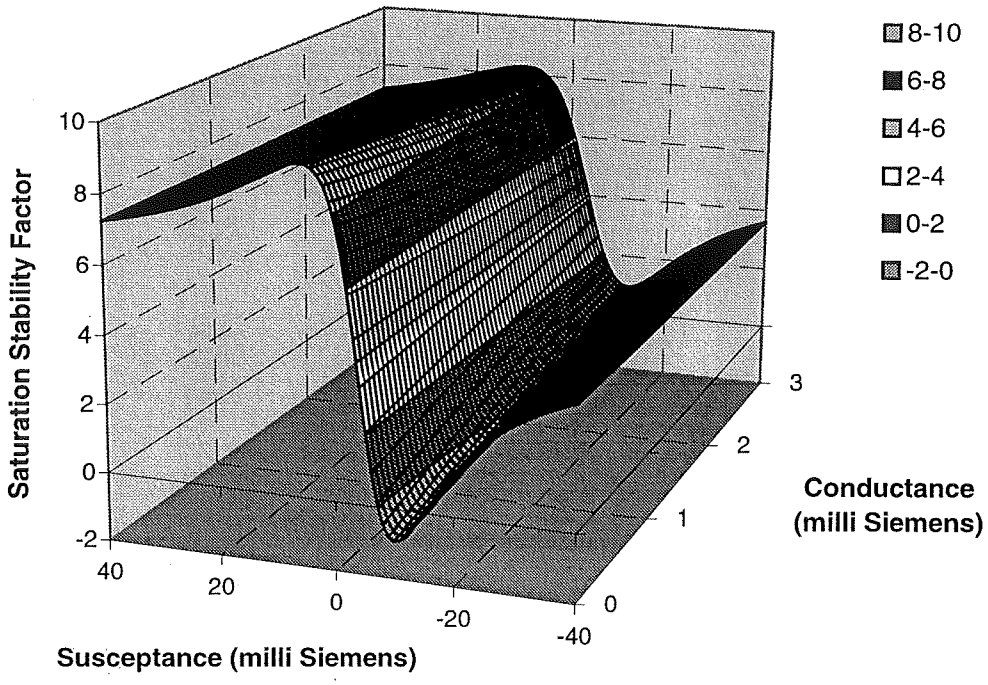


Figure C-4: *SSF* versus Z_{acp} (Base case: R_{acn} = 100 ohms, $1/Z_{dch}$ = 0+ j10 milli Siemens)

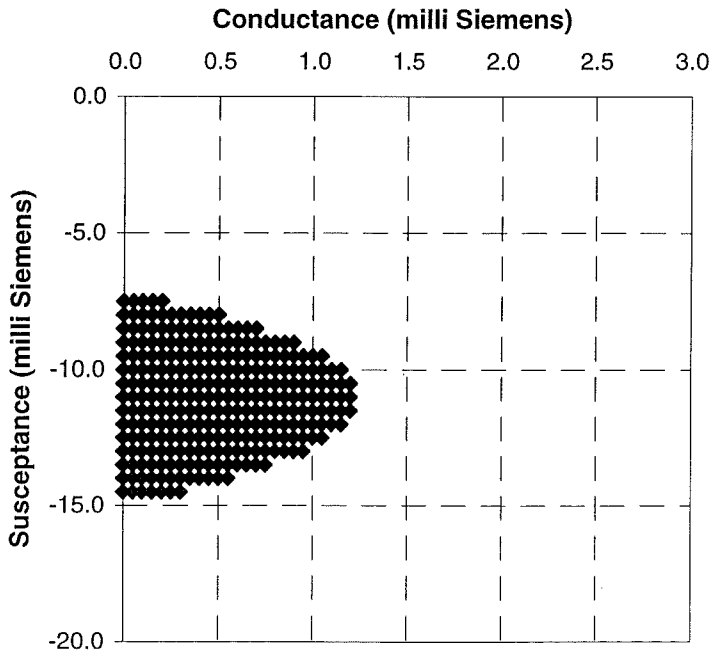
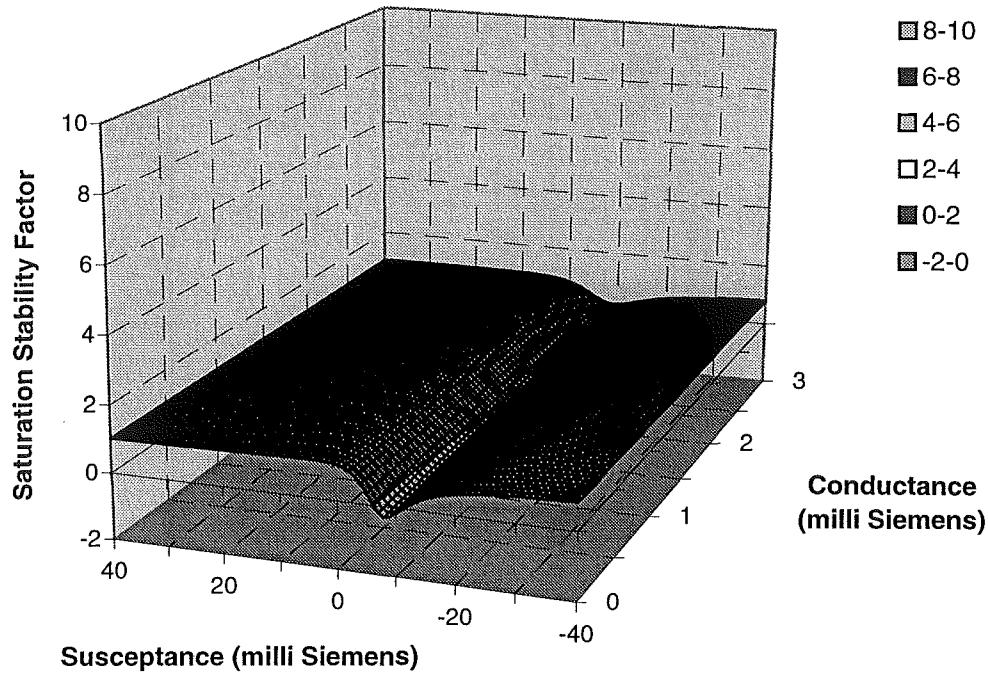
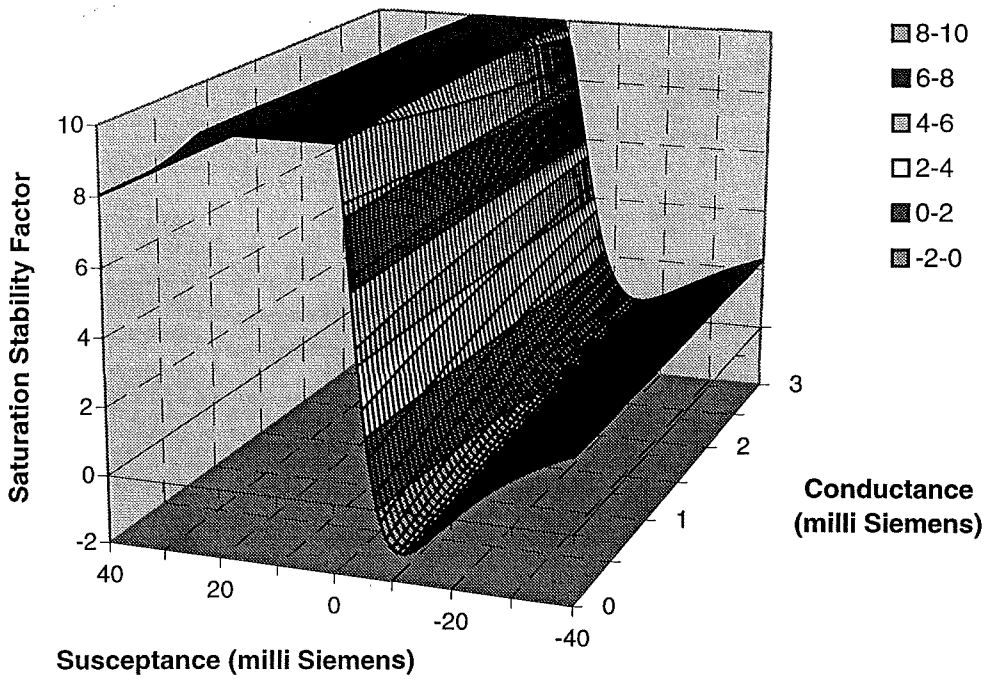


Figure C-5: Range of unstable Z_{acp} (Base case: R_{acn}= 100 ohms, $1/Z_{dch}$= 0+j10 milli Siemens)



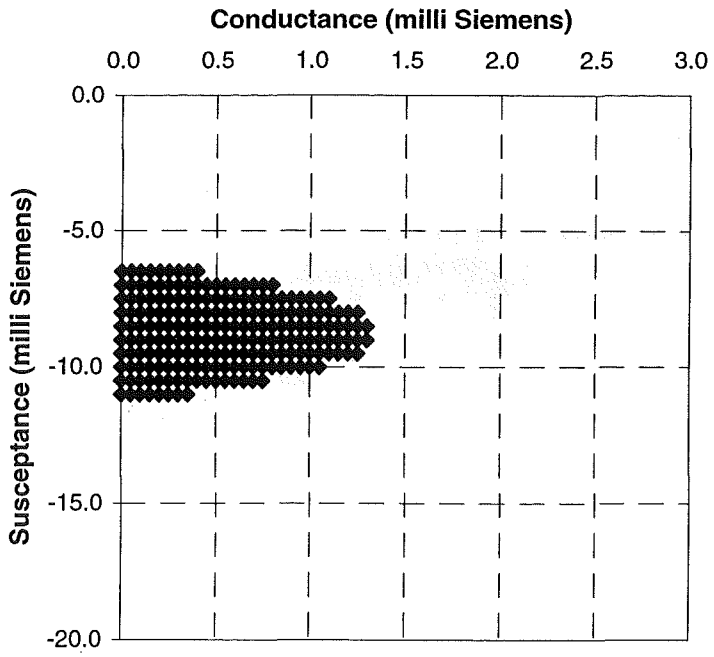
(i) Lower R_{acn} (R_{acn} = 10 ohms)



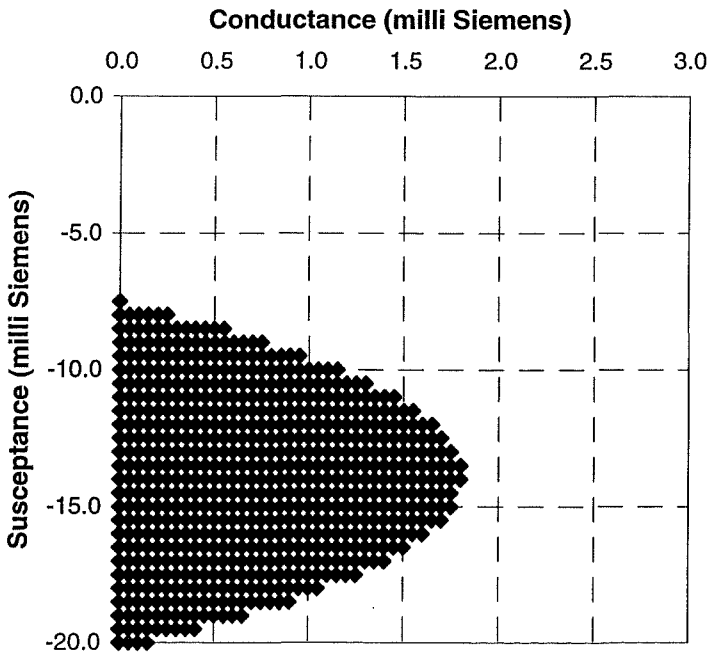
(ii) Higher R_{acn} (R_{acn} = 200 ohms)

Figure C-6: *SSF* versus Z_{acp} with different R_{acn}

When the dc side fundamental frequency impedance Z_{dch} is made inductive, the *SSF* surface becomes a mirror image of that when Z_{dch} is capacitive. Comparing Figure C-8i with that of the base case of Figure C-4, the minimum and maximum *SSF* occur on the opposite halves of the susceptance. However the *SSF* remains positive throughout the range of Z_{acp} which suggests that the system will always be stable when Z_{dch} is low and inductive.



(i) Lower R_{acn} (R_{acn} = 10 ohms)

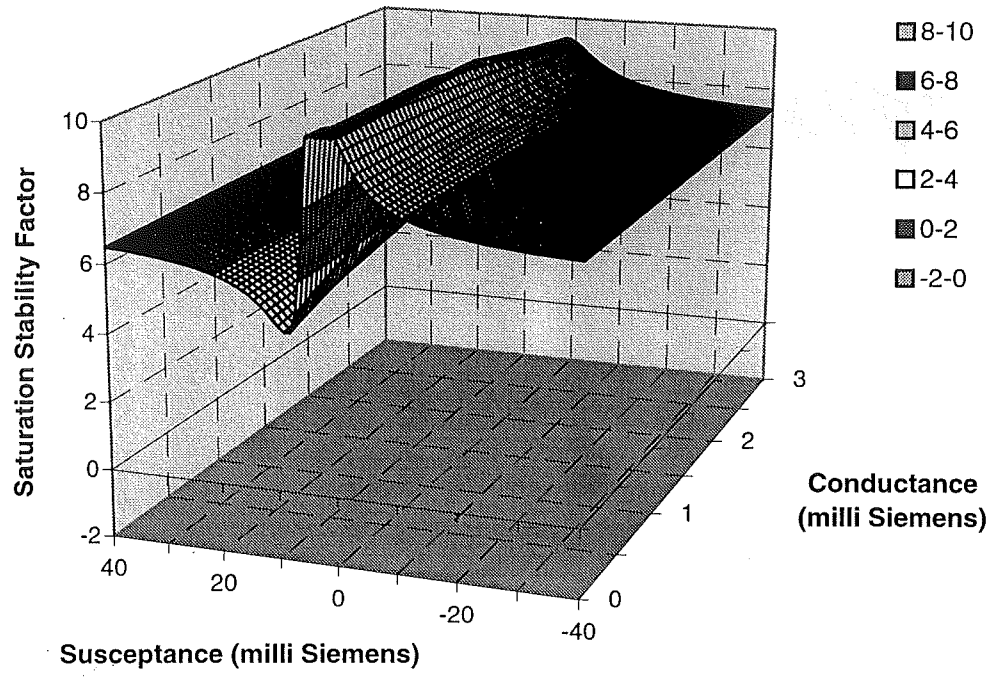


(ii) Higher R_{acn} (R_{acn} = 200 ohms)

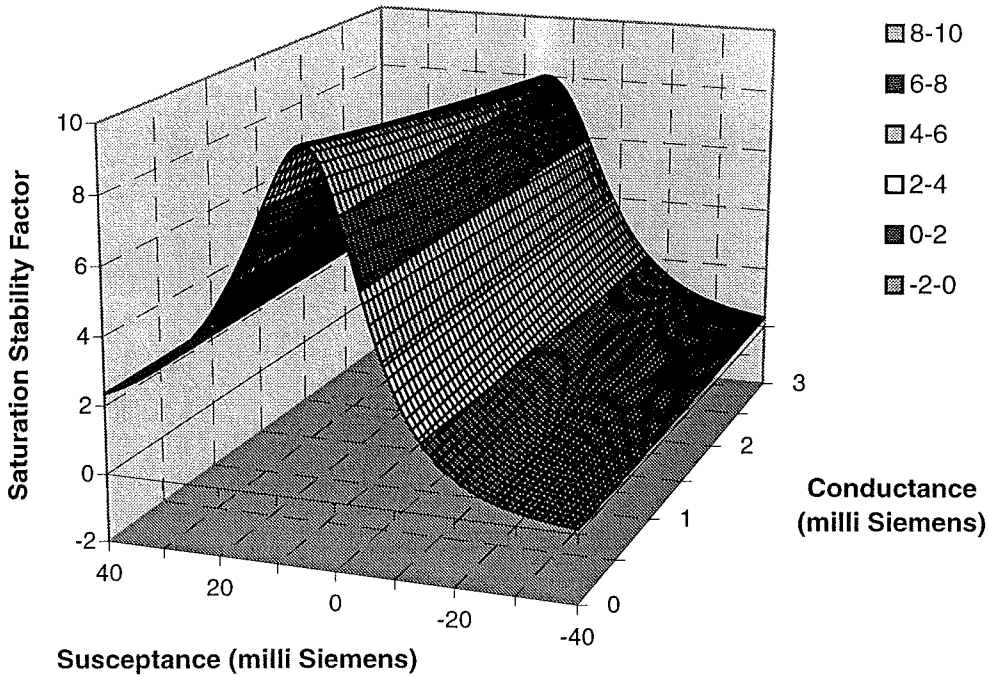
Figure C-7: Range of unstable Z_{acp} with different R_{acn}

If Z_{dch} is made slightly less capacitive by raising its susceptance to +j30.0 milli Siemens, the entire *SSF* versus Z_{acp} surface is shifted upwards, diminishing the unstable Z_{acp} region, as shown in Figure C-8ii. This leads to the conclusion that the characteristics of Z_{dch}, particularly its reactive property, play an important role in determining the relationship between *SSF* and

Z_{acp}. Unless Z_{dch} is capacitive the system *SSF*, and hence susceptibility to core saturation instability, is independent of Z_{acp}.



(i) Inductive dc side ($1/Z_{dch}$ = 0-j10 milli Siemens)



(ii) Less capacitive dc side ($1/Z_{dch}$ = 0+j30 milli Siemens)

Figure C-8: *SSF* versus Z_{acp} with different Z_{dch}

C.4 DC side fundamental frequency impedance

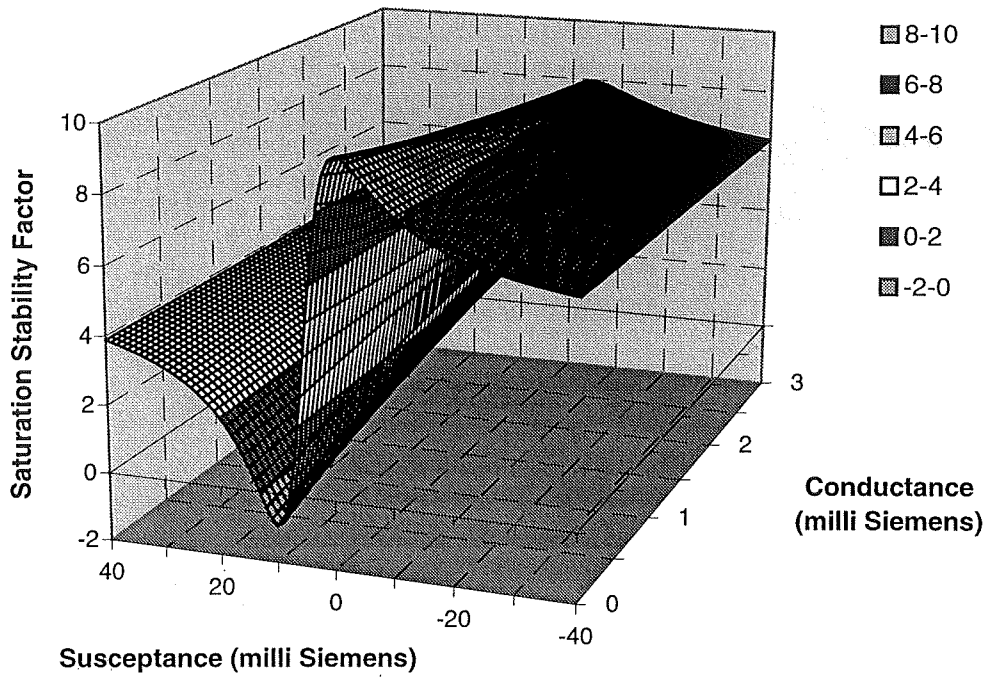


Figure C-9: *SSF* versus Z_{dch} (base case: R_{acn} = 100 ohms, $1/Z_{acp}$ = 1+j10 milli Siemens)

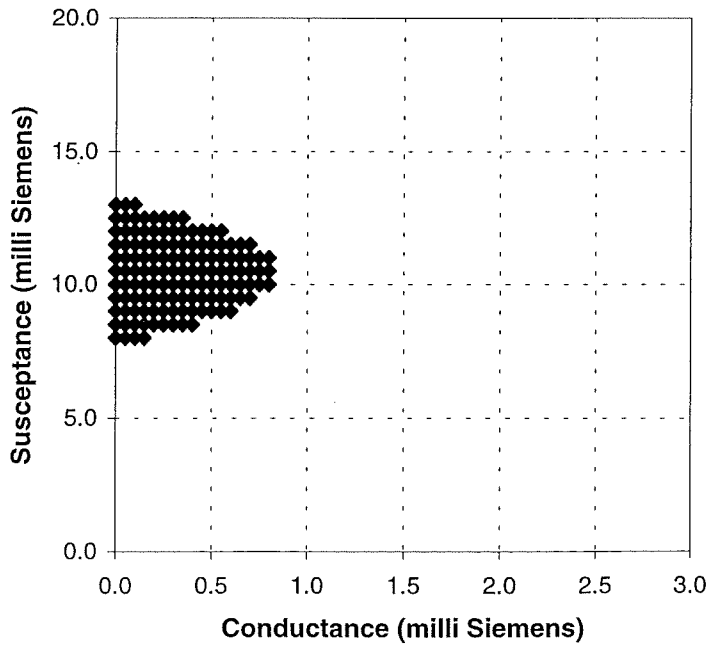


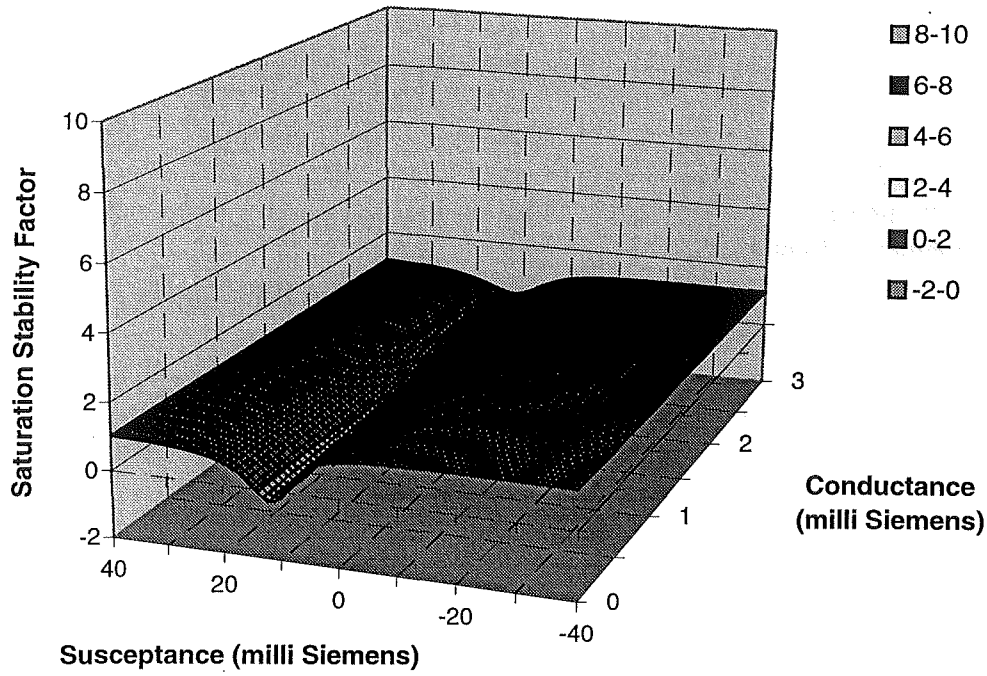
Figure C-10: Range of unstable Z_{dch} (Base case: R_{acn}=100 ohms, $1/Z_{acp}$=1-j10 milli Siemens)

With R_{acn} and Z_{acp} tuned to their respective unstable values, the relationship between *SSF* and Z_{dch} (dc side fundamental frequency impedance) as described in Chapter 4 is as shown in Figure C-9. The *SSF* varies considerably with the susceptance especially at low conductances. The range of unstable Z_{dch} indicated by negative *SSF* was confined to the area with low conductances and positive susceptances around 10 milli Siemens as shown in Figure C-10. This shows the presence of a series resonance on the dc side at a frequency slightly higher than the fundamental frequency.

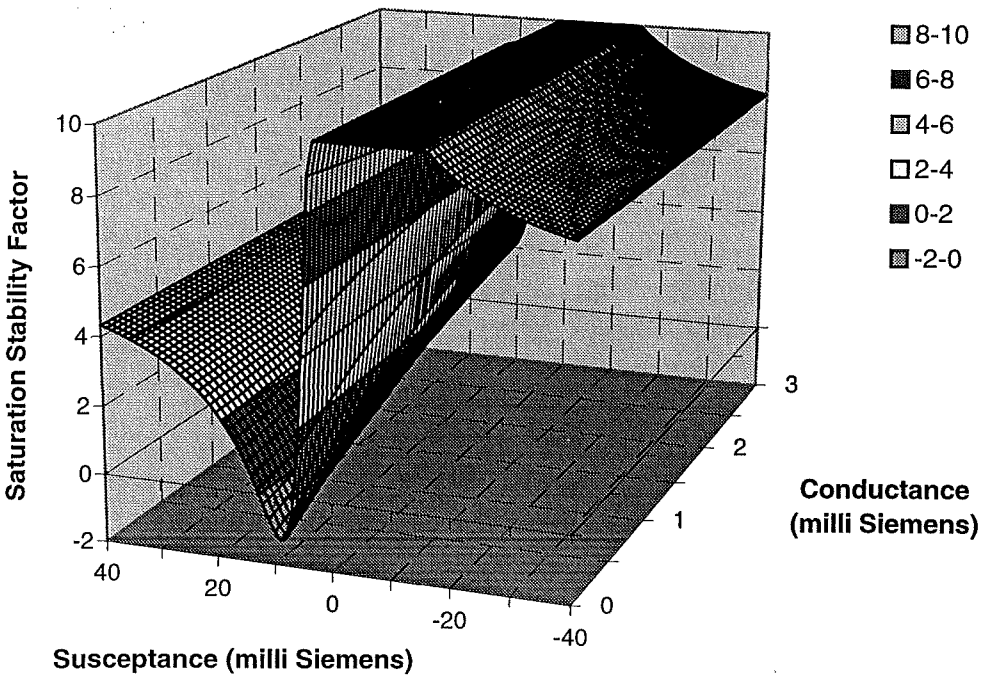
This relationship between *SSF* and Z_{dch} is tested with different values of R_{acn} and Z_{acp}. Figure C-11 shows the impact of low and high R_{acn} on the relationship between *SSF* and Z_{dch}. With low R_{acn}, the *SSF* surface is mostly flat with a value of 1 and the variation in *SSF* over the range of Z_{dch} considered is small. This shows a similar effect as shown earlier for the variation of Z_{acp} (Figure C-6), such that low R_{acn} lessens the influence of Z_{dch} on the *SSF*. Conversely, a high R_{acn} amplifies the impact of Z_{dch} on *SSF* with a significant increase in the variation of *SSF* with Z_{dch}. However, the unstable range of Z_{dch} is still confined to a region with low conductances and low positive susceptances. This confirms the original conclusion that the presence of a series resonance on the dc side at a frequency slightly higher than the fundamental frequency plays an essential part in the development of the instability irrespective of the value of R_{acn}. Figure C-12i and ii show the range of unstable Z_{dch} with low and high R_{acn} respectively. With low R_{acn}, the unstable region spreads over a greater range of conductance, whereas a high R_{acn} sees this region to cover a larger range of susceptance.

If Z_{acp} is made capacitive by raising its susceptance to +10 milli Siemens, the relationship between *SSF* and Z_{dch}, as shown in Figure C-13I, becomes the opposite to that of the base case when Z_{dch} is inductive. Moreover, the variation in *SSF* has reduced and it remains positive throughout the range of Z_{dch} considered. This implies that the influence of Z_{dch} is negligible when Z_{acp} is capacitive and that the system will always remains stable as long as Z_{acp} remains capacitive.

On the other hand if Z_{acp} is made slightly less inductive by lowering its susceptance to -30 milli Siemens, the *SSF* versus Z_{dch} surface remains very similar to that of the base case. There is still a significant amount of variation in *SSF* with Z_{dch} at this value of Z_{acp}. Furthermore, the unstable range of Z_{dch} is still congregated around low conductances and around positive susceptances of about +20 milli Siemens. This implies that as long as Z_{acp} is not capacitive, Z_{dch} will have a significant influence on the system *SSF* and stability. Figure C-14 shows the new range of unstable Z_{dch} with the less inductive Z_{acp} on the ac side.

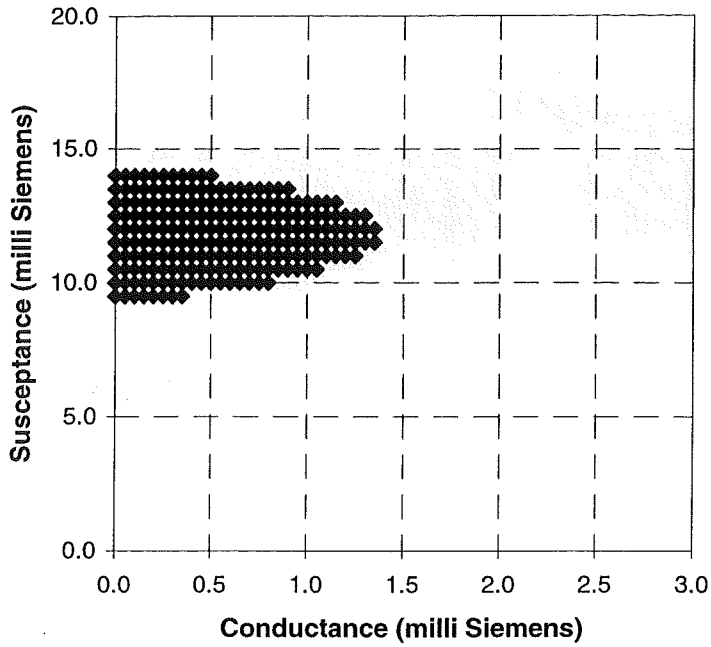


(i) Lower R_{acn} (R_{acn} = 10 ohms)

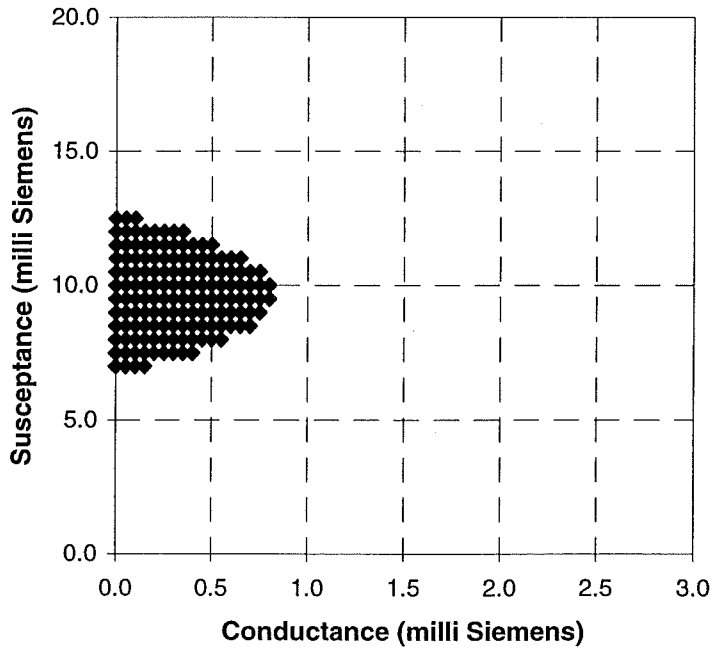


(ii) Higher R_{acn} (R_{acn} = 200 ohms)

Figure C-11: *SSF* versus Z_{dch} with different R_{acn}

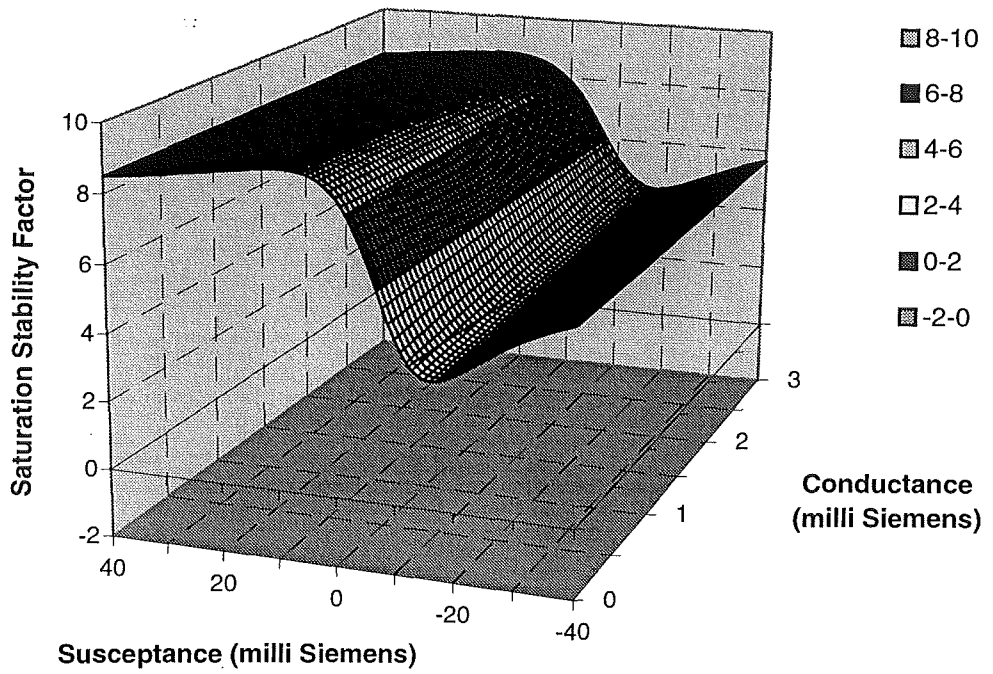


(i) Lower R_{acn} (R_{acn} = 10 ohms)

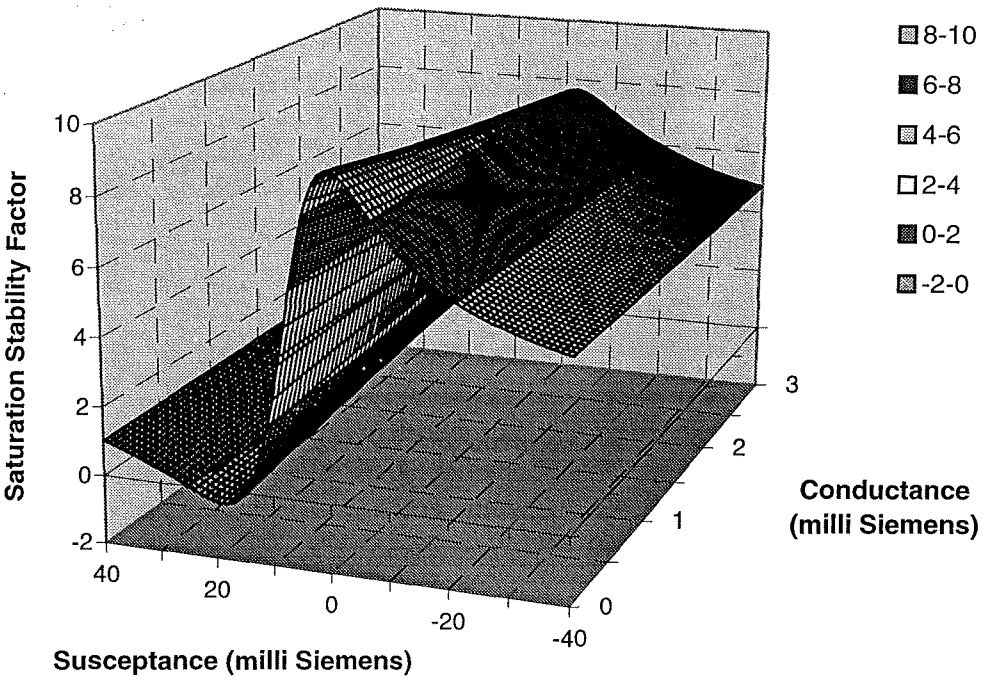


(ii) Higher R_{acn} (R_{acn} = 200 ohms)

Figure C-12: Range of unstable Z_{dch} with different R_{acn}



(i) Capacitive ac side ($1/Z_{acp}$ = 0+j10 milli Siemens)



(ii) Less inductive ac side ($1/Z_{acp}$ = 0-j30 milli Siemens)

Figure C-13: *SSF* versus Z_{dch} with different Z_{acp}

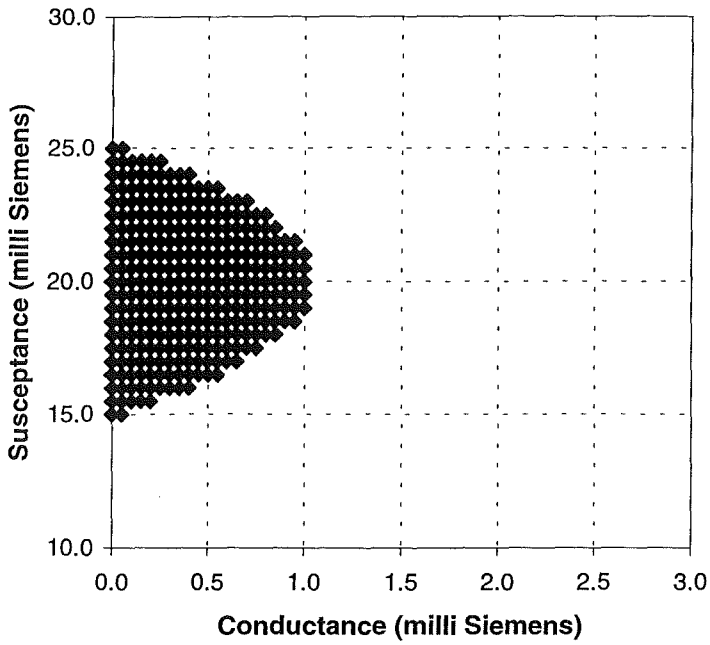


Figure C-14: Range of unstable Z_{dch} with less inductive Z_{acp}

C.5 Conclusion

The analysis above has clearly illustrated the level of influence that each of the harmonic impedances has on the *SSF* and system susceptibility to core saturation instability. The effect of R_{acn} on *SSF* is highly dependent on the characteristics of Z_{acp} and Z_{dch}. Furthermore, although changes in R_{acn} will affect the extent of variation in *SSF* with Z_{acp} and Z_{dch}, the unstable ranges of these two latter impedances with negative *SSF* remain relatively intact. Therefore, R_{acn} is considered the least significant factor among these impedances.

Z_{acp} and Z_{dch} are observed to equally affect each other's relationship with *SSF*. However the impact on the Z_{acp} relationship by making Z_{dch} less capacitive is far more pronounced as compared to the impact on Z_{dch} relationship when Z_{acp} is made less inductive (i.e. the changes in the *SSF* surface from that of the base case to that in Figure C-8 is far more significant than to that in Figure C-13). Therefore, it is anticipated that Z_{dch} will have a greater impact on the *SSF* than Z_{acp}.

Appendix D

Validation of effect of system impedances on Saturation Stability Factor

D.1 Introduction

The influence of HVDC system impedances on the *Saturation Stability Factor* are described in Chapter 4 and Appendix C. The main properties derived from the evaluation of the *SSF* are now validated with dynamic simulations.

The test system used for the verification of the *SSF* approach in Chapter 3 is used here to validate the effect of the system impedances on the system *SSF*. However, only the kicked-started type of core saturation instability is used in these simulations. The reason is that this case constitutes a more strenuous test and requires less simulation time. If a system can sustain kicked-started type of core saturation instability, it is most likely to be immune from its spontaneous counterpart.

D.2 Effect of AC side resistance at 0 Hz

A HVDC system has been found to be more vulnerable to core saturation instability if its ac side resistance at or near 0 Hz is high. Table D-1 shows the two test cases used to demonstrate this behaviour.

Test case	**1**	**2**
R_{acn} **(ohms)**	200	400
R1 (ohms)	200	400
SSF	0.25	- 0.78

Table D-1: Test cases for validation of effect of R_{acn} on *SSF*

Test case 1 has a resistance R_{acn} of 200 ohms and the corresponding *SSF* is positive at 0.25. This implies that the system will be stable as confirmed by the EMTDC simulation results of Figure D-1. On the contrary, the R_{acn} of test case 2 has been doubled and the resulting *SSF* is negative at -0.78. Figure D-2 shows the growth of the instability from a low level of initial saturation. Both cases were started with the same initial conditions that is a similar level of core saturation at the end of the inducing firing angle modulation which occurs after 1.5 seconds. The level of core saturation is defined by the amount of negative sequence dc distortion on the transformer magnetising current. The inducing modulation is then selected so that this distortion level is similar in both cases. This approach is used in all the simulations described in this appendix.

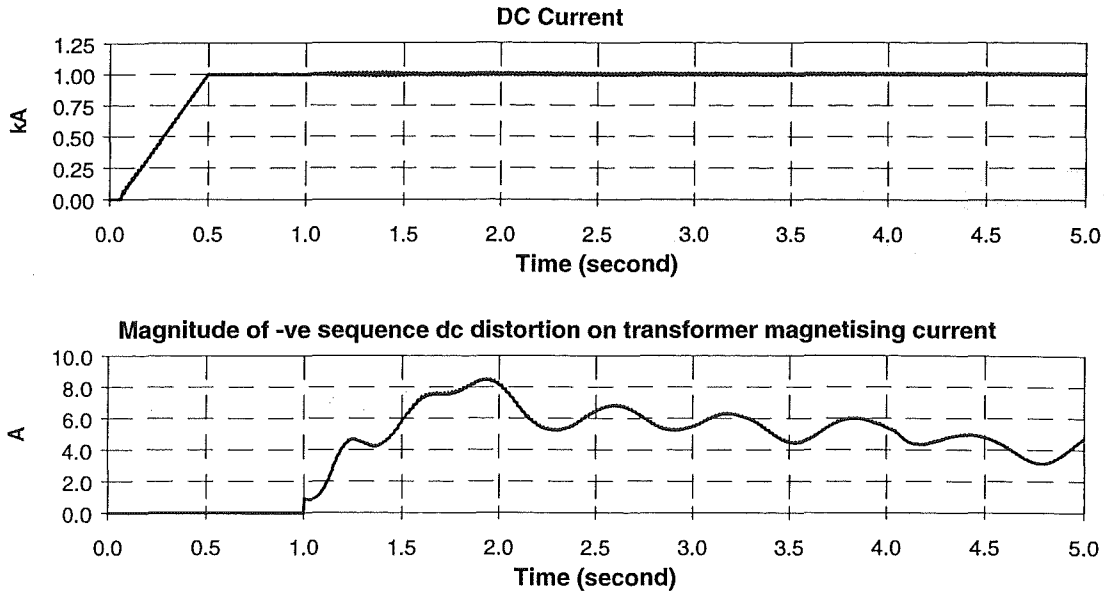


Figure D-1: Simulation results of test case 1 for validation of R_{acn} effect

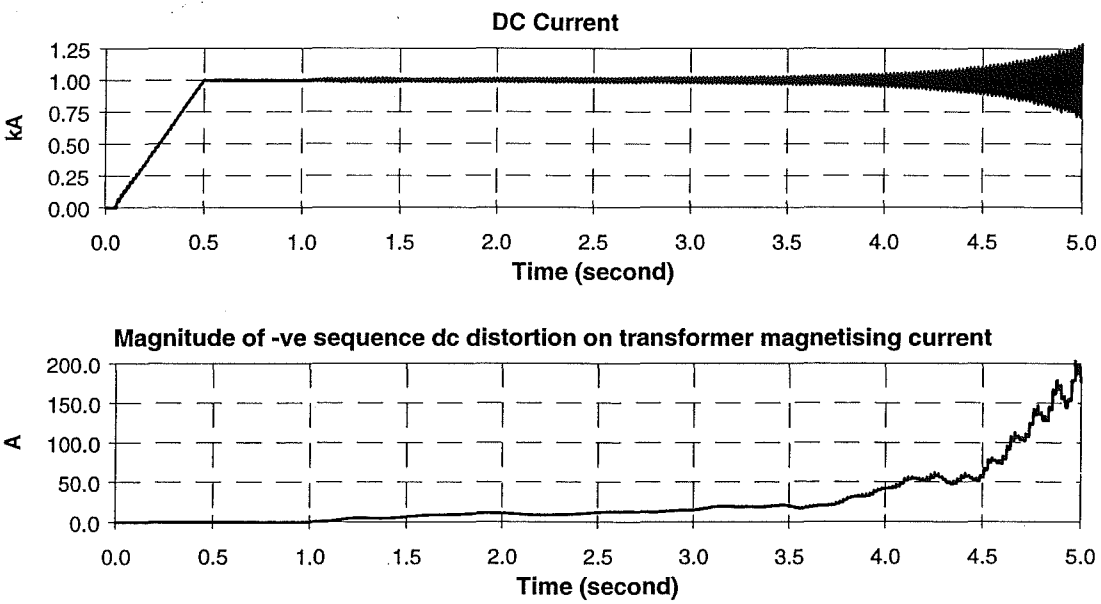


Figure D-2: Simulation results of test case 2 for validation of R_{acn} effect

D.3 Effect of AC side second harmonic impedance

The effect of the ac side second harmonic impedance was found to be more complicated compared to that of the resistance described in the previous section. Both the active and reactive parts of the impedance or admittance were found to significantly affect the system *SSF* and hence the system vulnerability to this instability. Four test cases are used to demonstrate the observations made from the *SSF* viewpoints in the previous chapters. Details of these test cases are given in Table D-2.

Test case	1	2	3	4
AC side second harmonic admittance (milli Siemens)	1.0 - j 10.0	1.0 + j 10.0	1.0 - j 20.0	2.0 - j 10.0
R2 (ohms)	1030.0	975.35	1061.2	513.79
L2 (mH)	6.42	6.57	6.01	6.18
C2 (μF)	378.92	401.96	390.28	394.00
SSF	- 0.11	8.76	1.42	0.55

Table D-2: Test cases for validation of effect of Z_{acp} on *SSF*

Test case 1 with negative *SSF* of -0.11 is taken as the base case and the corresponding instability is clearly evident in the simulation result of Figure D-3. At the end of the inducing firing angle modulation, the transformer is saturated with about 30 A of negative sequence dc current flowing in its magnetising inductance. After removal of the modulation, this saturating dc current continues to grow and accelerate, and causes an instability.

The other three cases are variants of case 1 used to illustrate the stabilising effect of changing either the conductance or susceptance of the system. In test case 2, the second harmonic impedance is capacitive whereas that in case 1 is inductive. The new *SSF* is very positive at 8.76 and the system is virtually immune to the instability. The inducing firing angle modulation hardly affected the dc current whereas the level of saturating dc current starts to decrease even before the removal of the modulation. In case 3, the ac side second harmonic impedance is made less inductive by doubling its susceptance. This alteration also results in a positive *SSF* and the simulation result shown in Figure D-5 confirms this prediction. Lastly in case 4, the ac side conductance at the second harmonic is doubled, making the *SSF* to become once again positive and the stability of the system is demonstrated by the simulation result in Figure D-6.

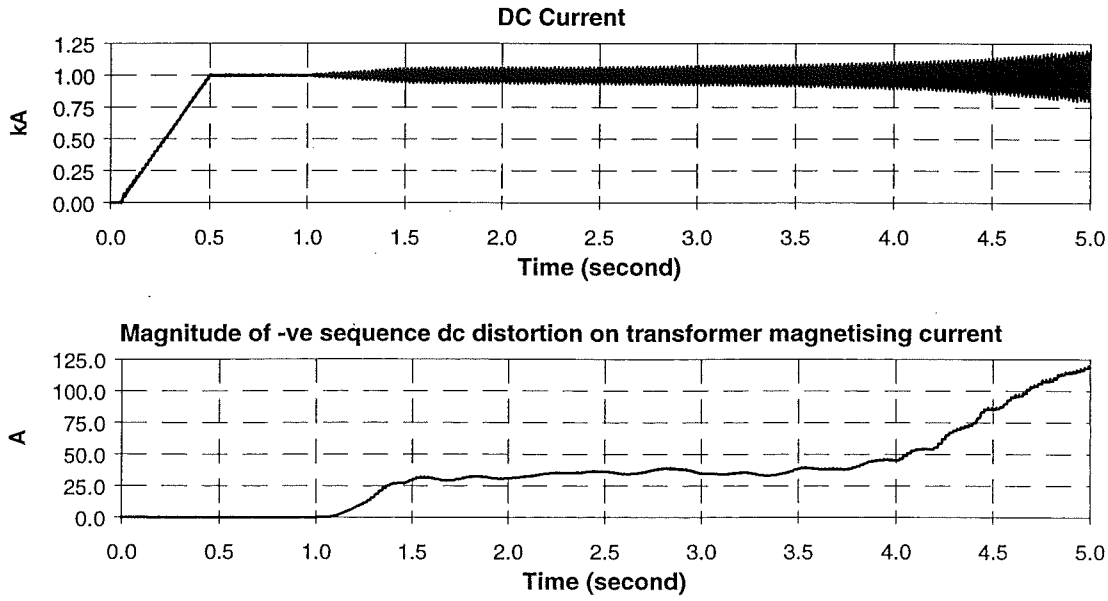


Figure D-3: Simulation results of test case 1 for validation of Z_{acp} effect

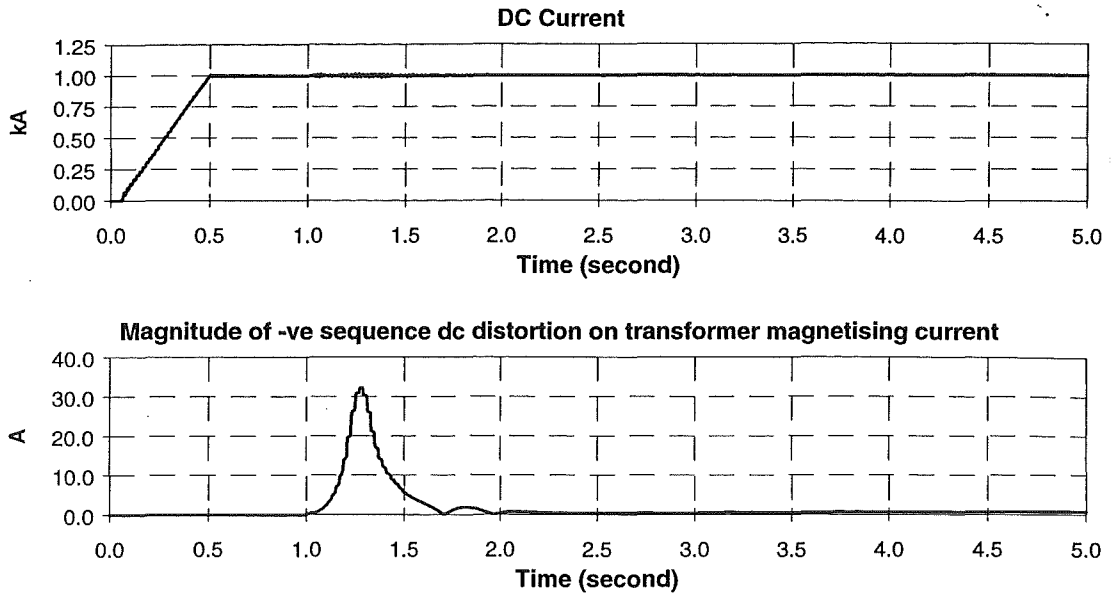


Figure D-4: Simulation results of test case 2 for validation of Z_{acp} effect

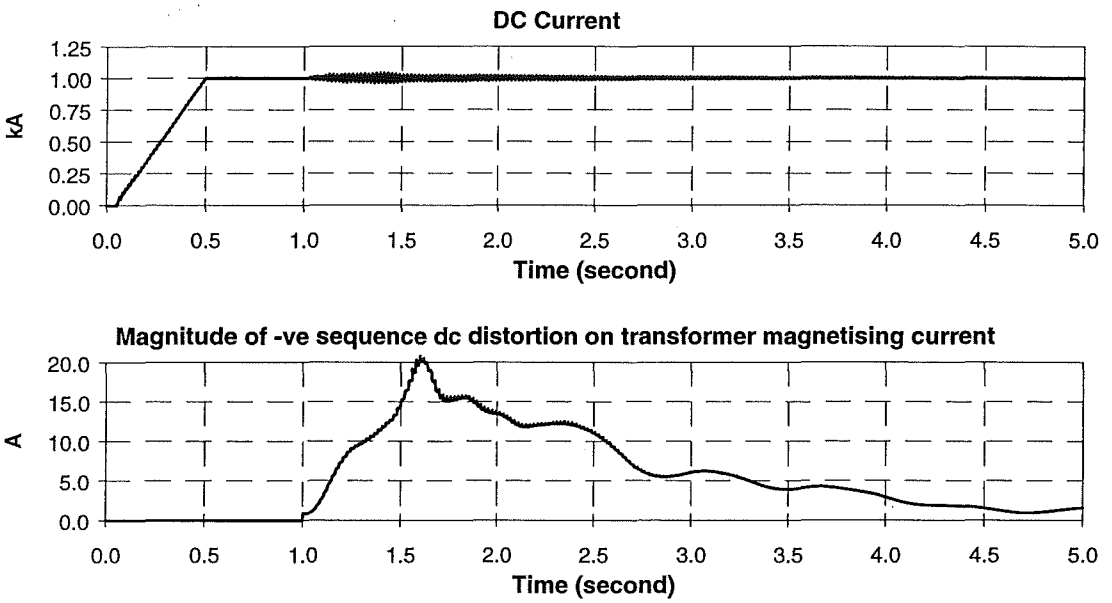


Figure D-5: Simulation results of test case 3 for validation of Z_{acp} effect

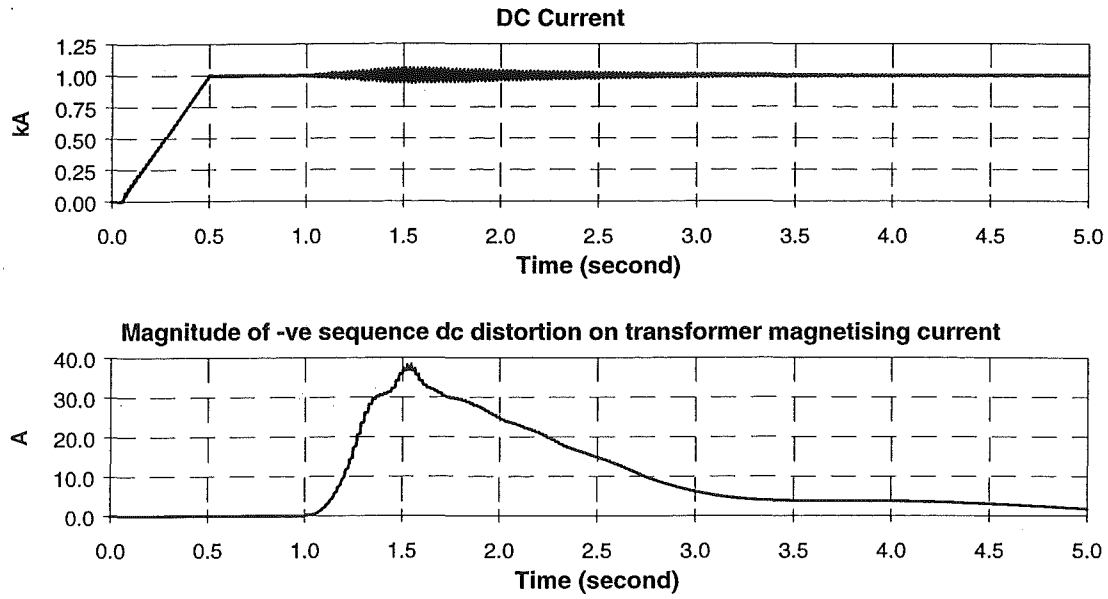


Figure D-6: Simulation results of test case 4 for validation of Z_{acp} effect

D.4 Effect of DC side fundamental frequency impedance

In Chapter 4, the dc side harmonic impedance at the fundamental frequency was found to exhibit significant influence on the system *SSF*. In this section, such prediction is validated with dynamic EMTDC simulations. Table D-3 details the test cases used in the simulations to verify the effect of Z_{dch}.

Case	1	2	3	4
DC side second harmonic admittance (milli Siemens)	0.0 + j 10.0	0.0 - j 10.0	0.0 + j 20.0	1.0 + j 10.0
R3 (ohms)	0.0	0.0	0.0	9.901
L3 (mH)	600.0	918.67	143.75	593.89
C3 (μF)	11.0334	16.8767	33.4495	11.1458
SSF	- 0.11	8.08	2.25	0.84

Table D-3: Test cases for validation of effect of Z_{dch} on *SSF*

Test case 1 is similar to that used for the validation of the effect of Z_{acp} in the preceding section. However, the results are repeated here for the ease of comparison. In test case 2, the impedance is changed from capacitive to inductive. The resultant *SSF* is positive at 8.08 indicating the stability of the system as shown in the simulation results in Figure D-8. Figure D-9 and Figure D-10 show the other two stable cases which have the dc side fundamental frequency susceptance doubled and the conductance raised respectively.

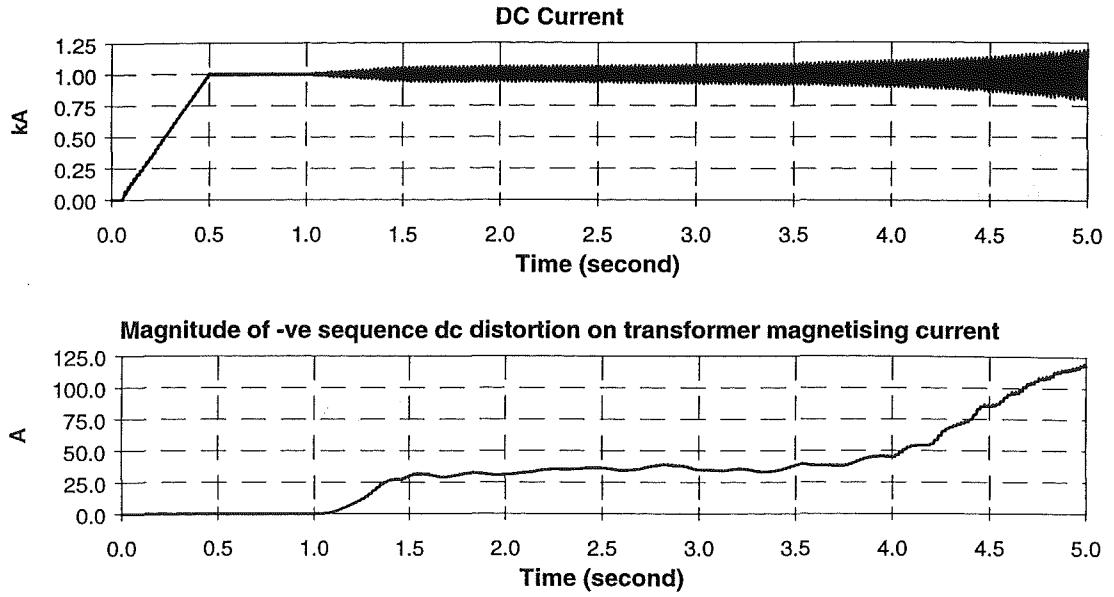


Figure D-7: Simulation results of test case 1 for validation of Z_{dch} effect

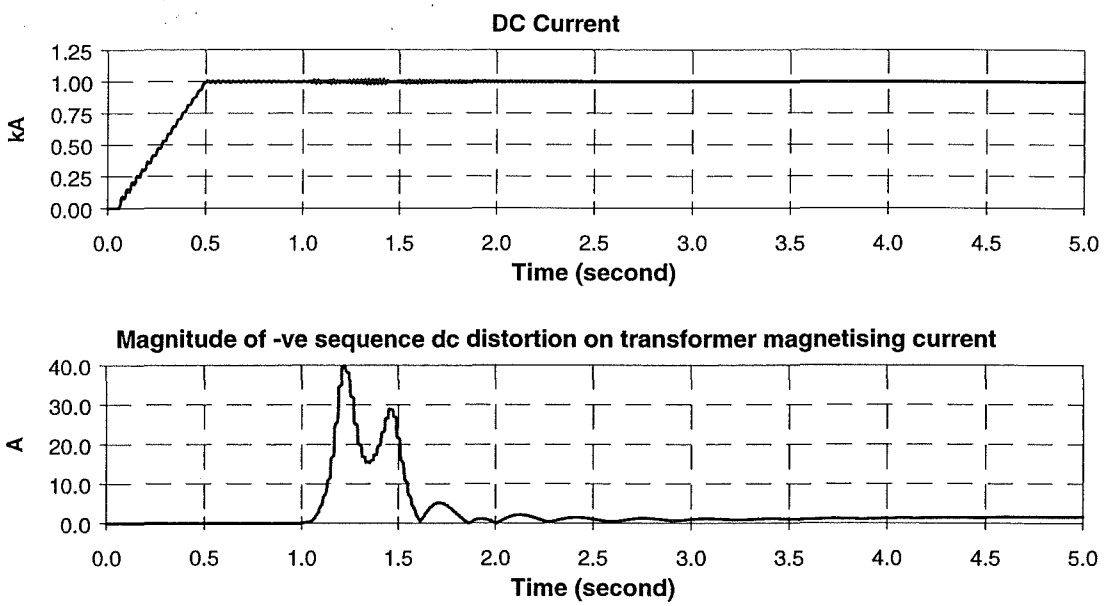


Figure D-8: Simulation results of test case 2 for validation of Z_{dch} effect

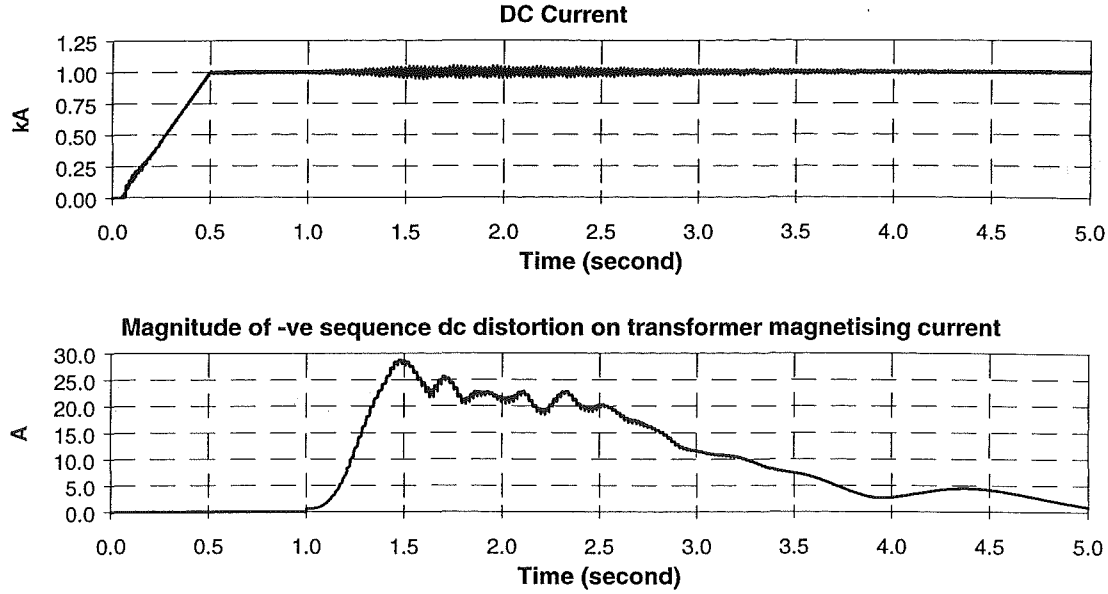


Figure D-9: Simulation results of test case 3 for validation of Z_{dch} effect

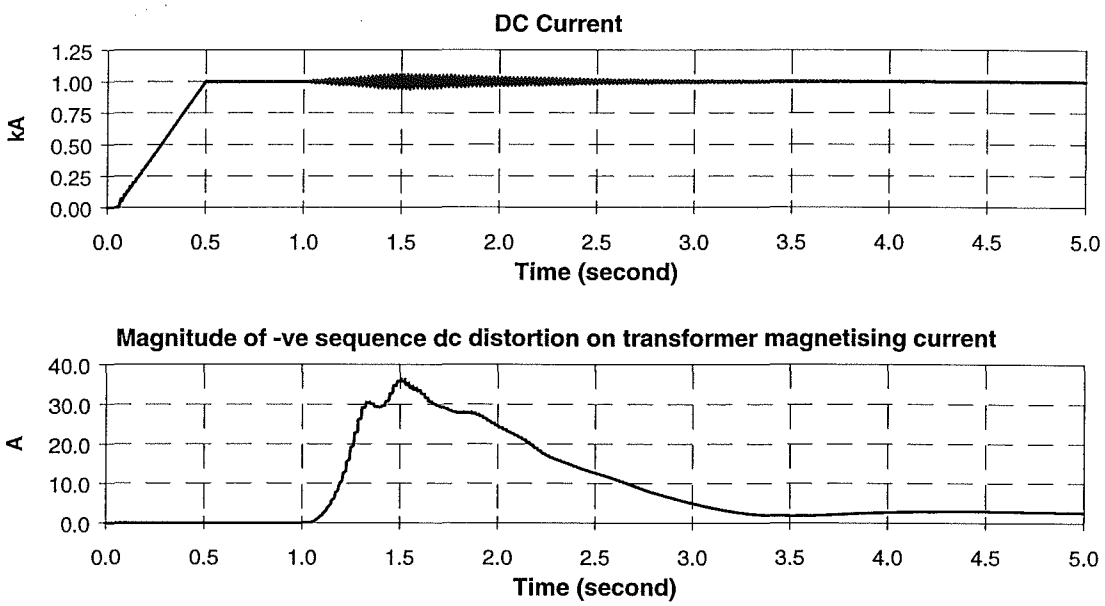


Figure D-10: Simulation results of test case 4 for validation of Z_{dch} effect

D.5 Conclusions

The EMTDC dynamic simulations described above have verified the deductions made from the *SSF* approach about the dependencies of the system susceptibility to core saturation instability on the system impedance profile. The close agreements observed with these two differing approaches confirm the conclusion that an HVDC system with such instability possesses the following impedance characteristics:

- A high and inductive ac side second harmonic impedance with a parallel resonance at a frequency near but higher than the second harmonic frequency.
- A low and capacitive dc side fundamental frequency impedance with a series resonance at a frequency near but higher than the fundamental frequency.
- A high resistance at or near 0Hz on the ac side,

Appendix E

Comparison of convertor controller response in different systems

E.1 Introduction

The effect of convertor controller on the *SSF* and the system susceptibility to core saturation instability were described in Chapter 4. In this section, this effect is extended to show that a small change in the system impedance can greatly alter the behaviour of the convertor controller. The deductions made from the evaluated *SSF* are validated with dynamic simulations using PSCAD/EMTDC.

E.2 Description of the test systems

The test system described in Appendix B and widely used throughout the thesis is modified to illustrate the effect of the convertor controller. Table E-1 gives the details of the two test systems used. Test case 1 is the base system used to compute the *SSF* in Chapter 4. In test case 2, the ac side second harmonic susceptance is halved to 5 milli Siemens and the corresponding RLC components are modified as shown in the table. The values of the second harmonic impedance components R2, L2 and C2 are almost the same in both cases.

Test case	**1**	**2**
AC side second harmonic admittance (milli Siemens)	1.0 - j 10.0	1.0 - j 5.0
R2 (ohms)	1030.0	1013.73
L2 (mH)	6.42	6.27
C2 (μF)	378.92	395.92

Table E-1: Description of the test systems used to illustrate the effect of convertor controller

Figures E-1 and E-2 show the *SSF* surface for the two systems plotted against the frequency response of the convertor controller. Despite the close similarity between the two systems, their *SSF*'s are quite different for the same range of control responses. This emphasises the importance of the system impedances to the controller's behaviour towards the instability.

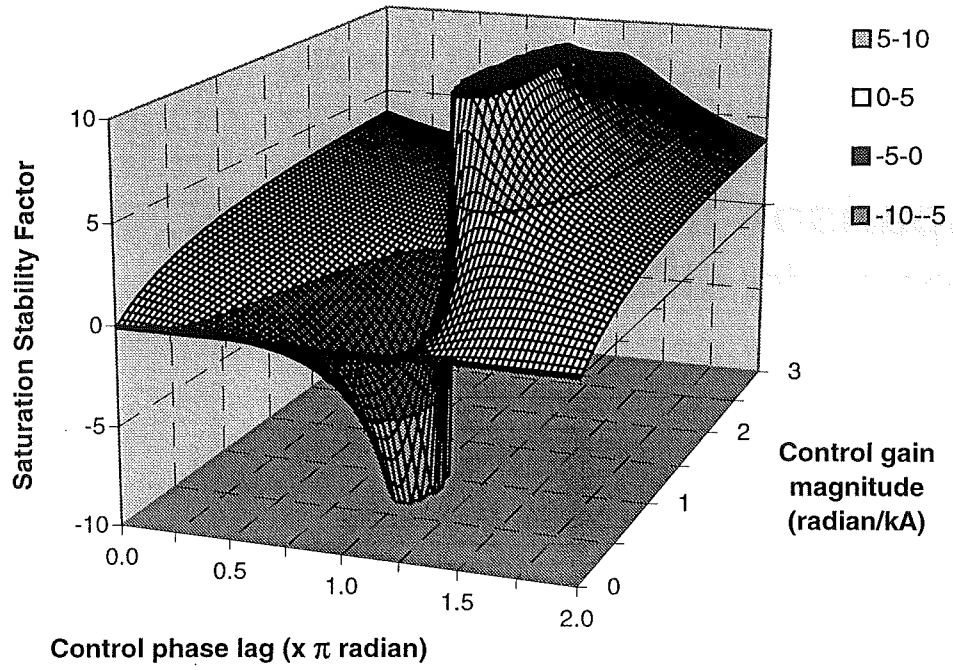


Figure E-1: *SSF* versus control responses for test system 1

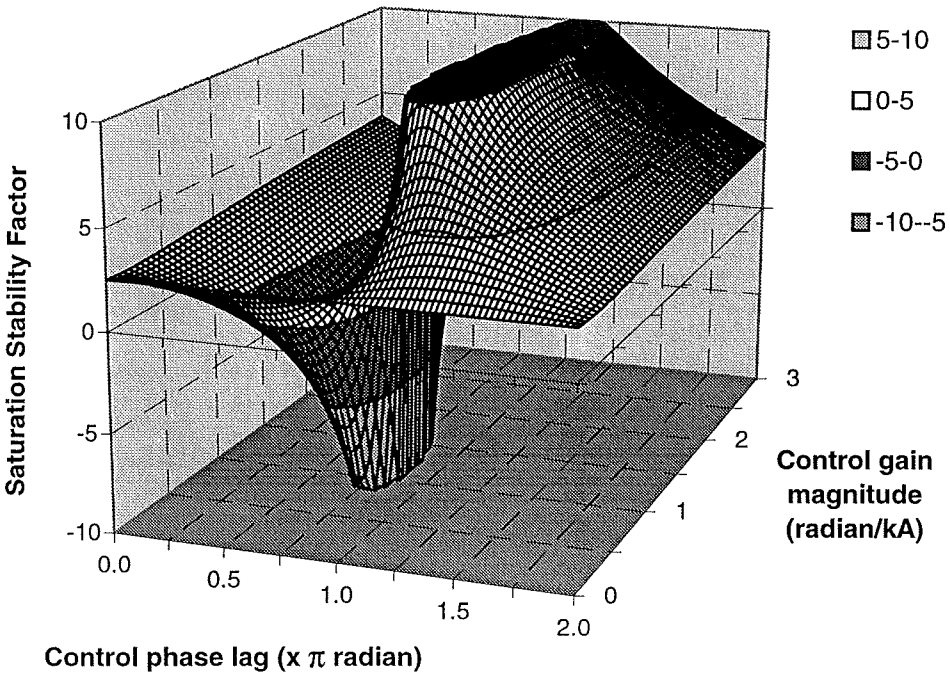


Figure E-2: SSF versus control responses for test system 2

From these figures, the ranges of control responses where the *SSF* is evaluated to be negative are illustrated with scatter plots in Figure E-3 and Figure E-4. It is obvious that some controller will be suitable for both systems and some will only be applicable in one system. These two ranges of unstable control responses are combined in Figure E-5 to illustrate the differences and similarities of their behaviours toward the instability.

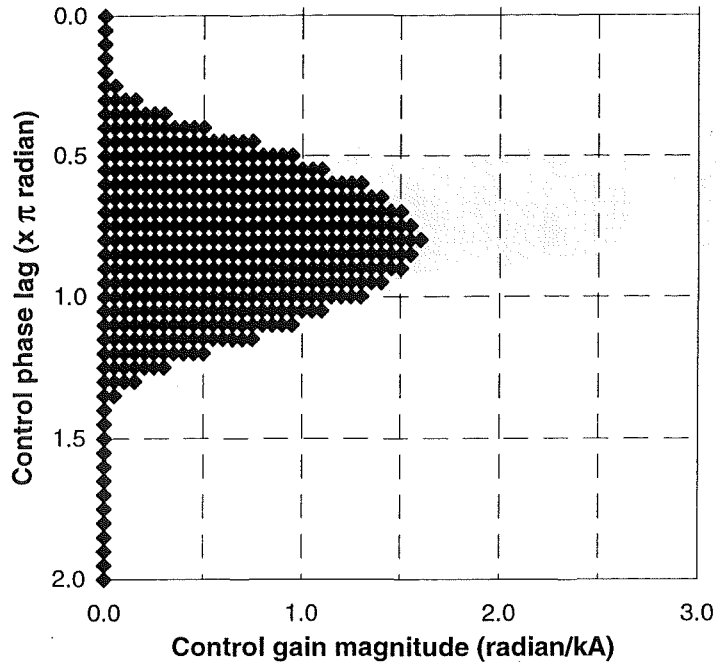


Figure E-3: Range of unstable control responses for test system 1

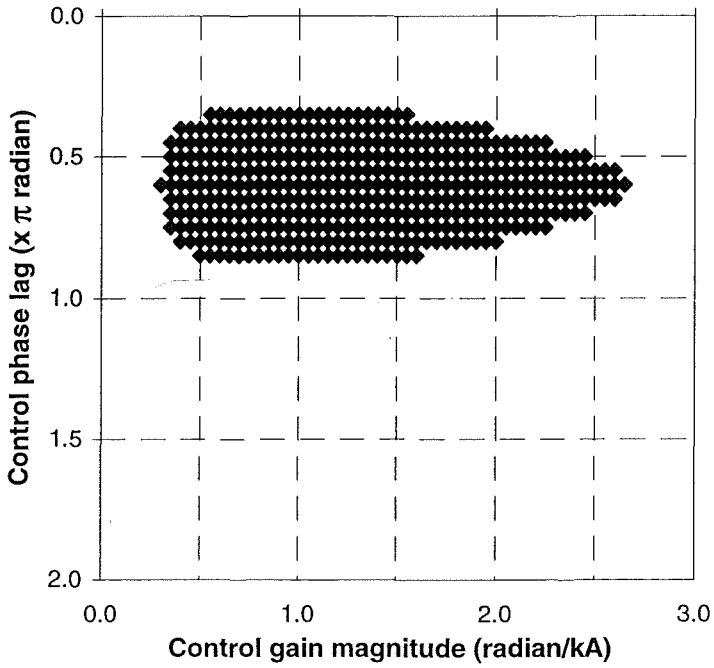


Figure E-4: Range of unstable control responses for test system 2

Four control responses, labelled A-D on Figure E-5, represent the controllers used in this demonstration. Only the proportional and integral type of controller is used the simulations. Details of the four controllers are given in Table E-2.

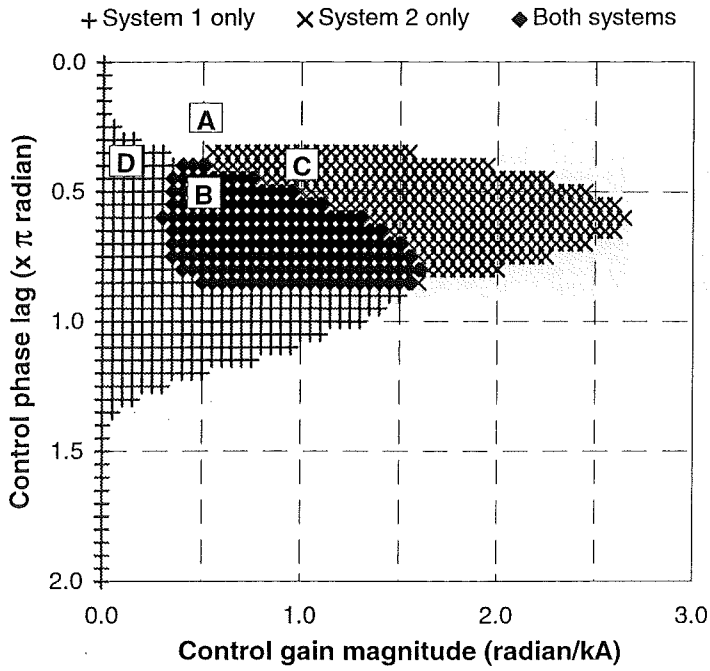


Figure E-5: Combined range of unstable control responses for both systems

Controller	A	B	C	D
Magnitude response (radian/kA)	0.50	0.40	1.0	0.10
Phase response (x π radian)	-0.10	-0.45	-0.40	-0.40
Proportional gain (radian/kA)	0.4755	0.0626	0.3090	0.0309
Integral time constant (kA-s/radian)	0.0206	0.0081	0.0033	0.0335
***SSF* for system 1**	1.37	-0.46	0.71	-0.25
***SSF* for system 2**	1.86	-0.40	-1.19	1.71

Table E-2: Description of the controllers used in the illustration

From the evaluated *SSF*, controller A is expected to exhibit stabilising effect on both test systems whereas controller B is destabilising. Controller C is applicable in system 1 but becomes unstable when applied to system 2. Lastly, controller D is anticipated to be suitable for system 2 but not for system 1.

E.3 Simulation results

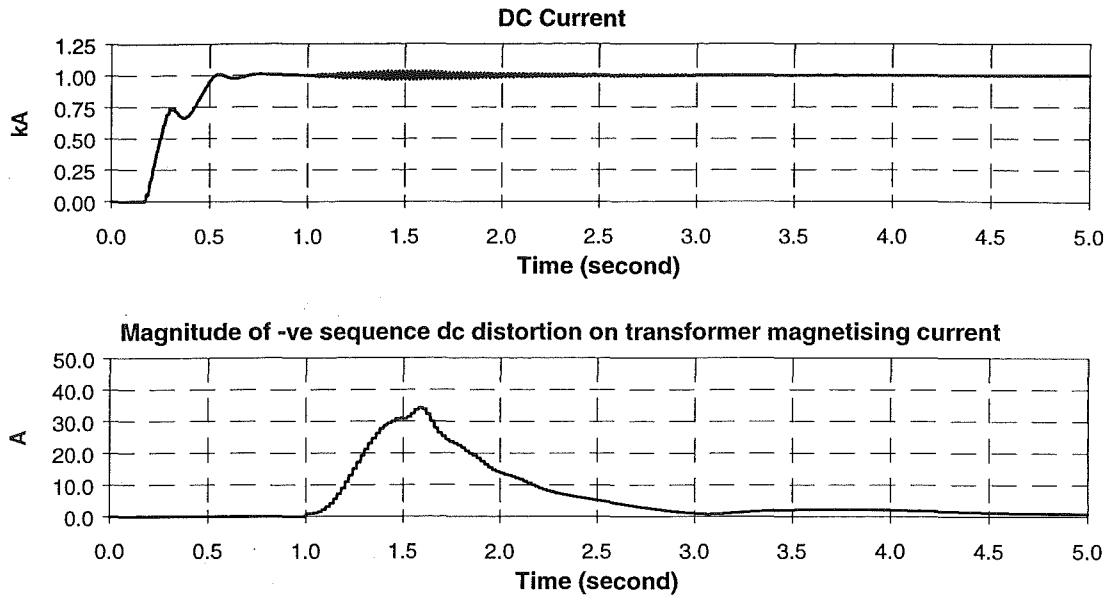


Figure E-6: Simulation results of controller A response in system 1

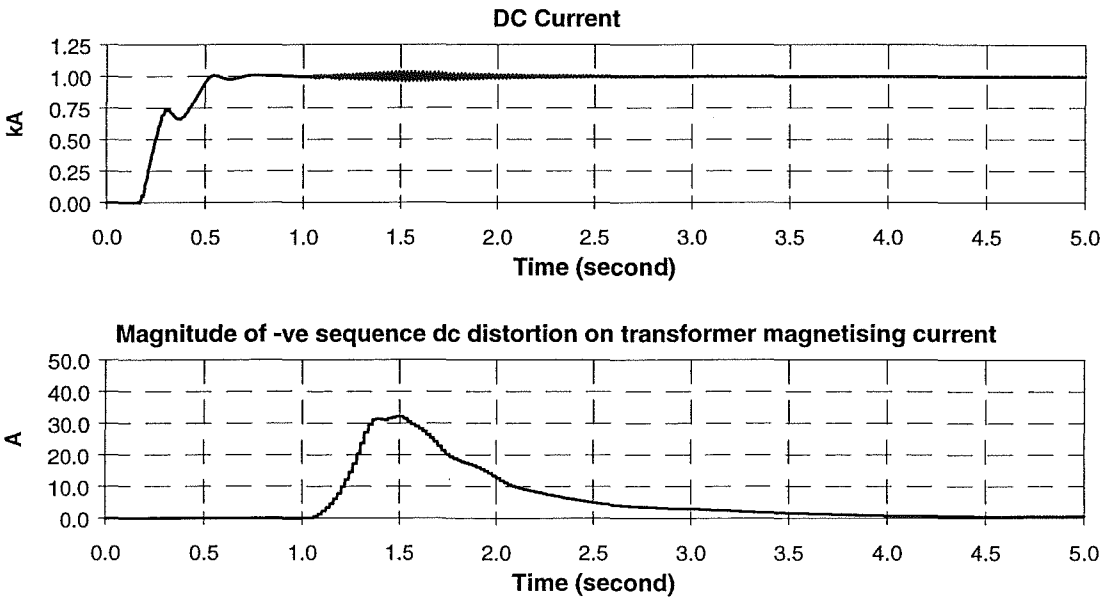


Figure E-7: Simulation results of controller A response in system 2

The EMTDC simulation results of Figures E-6 and E-7 show the stable response of controller A in both test systems. After the removal of the disturbing modulation on the convertor firing angle order at the time of 1.5 second, the distortions decayed away swiftly in just over one second.

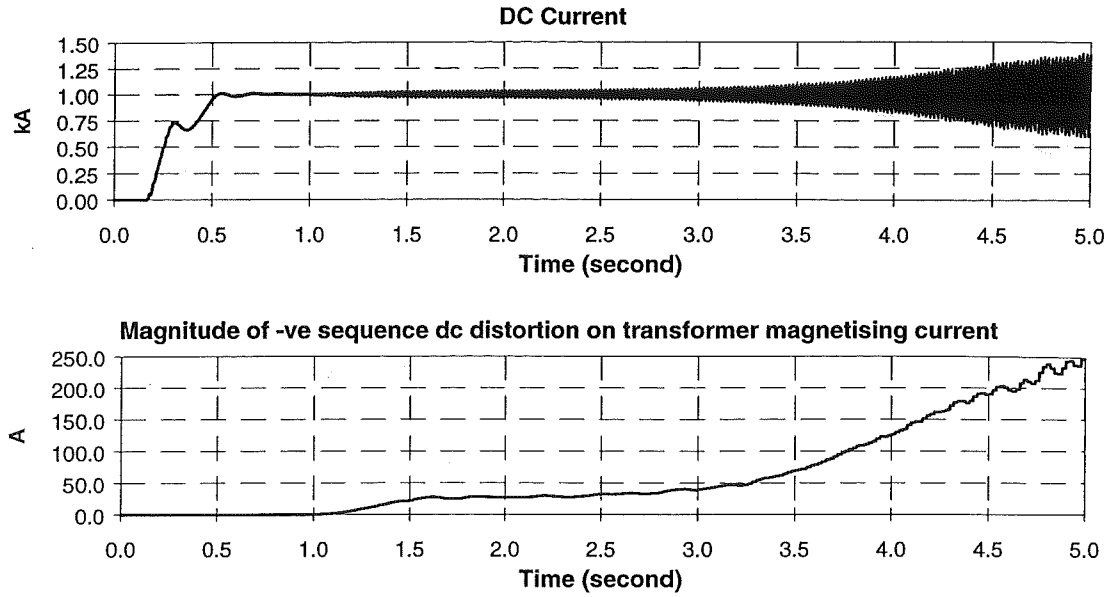


Figure E-8: Simulation results of controller B response in system 1

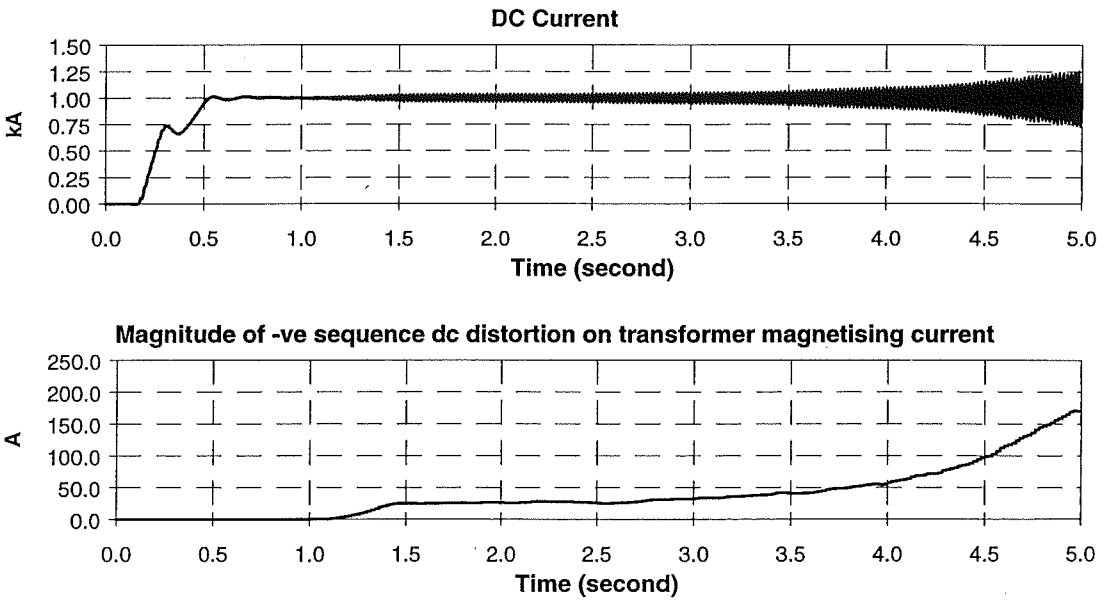


Figure E-9: Simulation results of controller B response in system 2

Figures E-8 and E-9 clearly show the development of the instability. In between the time of 1.0 and 1.5 second when firing angle modulation is introduced to the system, the magnitude of the saturating negative sequence dc current grows steadily to about 30 A. After the removal of the modulation, the rate of growth of this distorting current drops but quickly accelerates as the instability develops. Within the spate of 3 seconds, the low level of saturation has swelled to unprecedented levels with clear evidence of an instability.

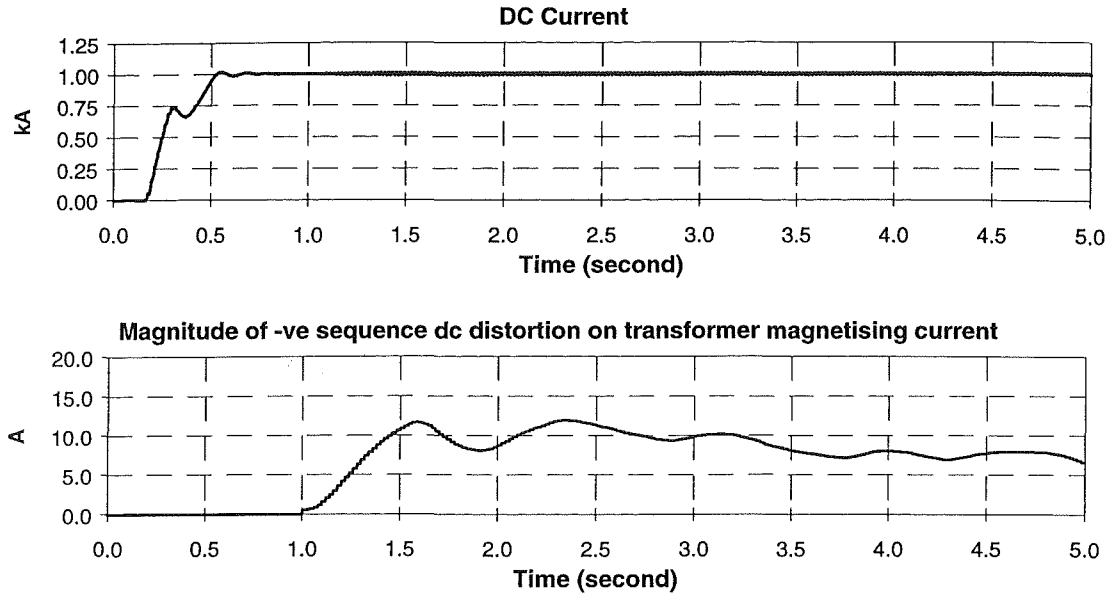


Figure E-10: Simulation results of controller C response in system 1

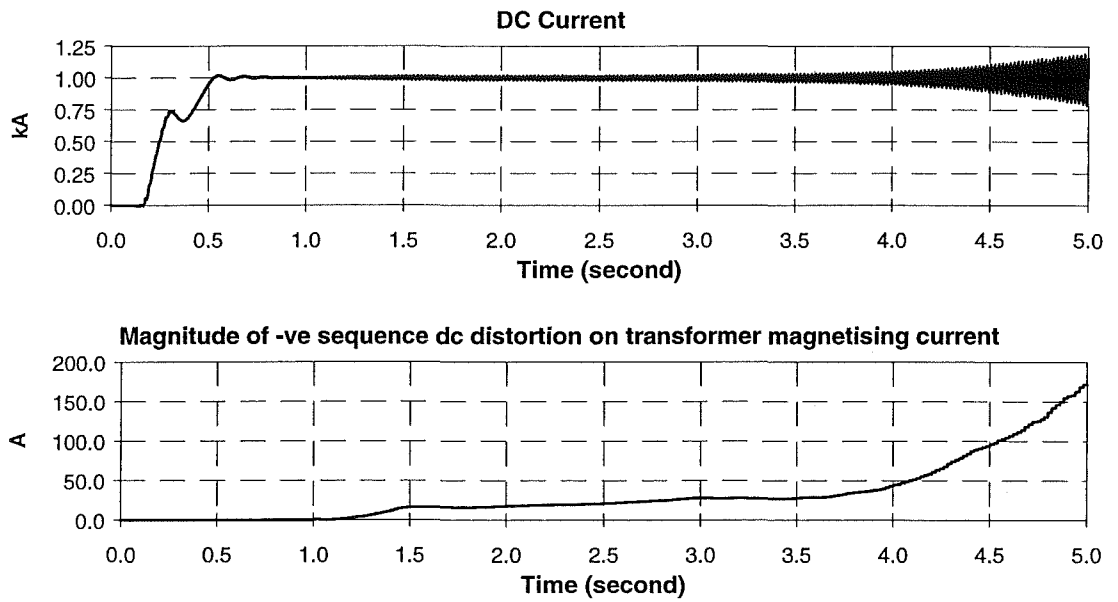


Figure E-11: Simulation results of controller C response in system 2

With convertor controller C, test system 1 is stable with positive *SSF*. This is verified by the simulation results of Figure E-10 although the rate of decay is very low. However, this particular controller is unsuitable for system 2. Figure E-11 shows the presence of the instability when controller C is used in system 2.

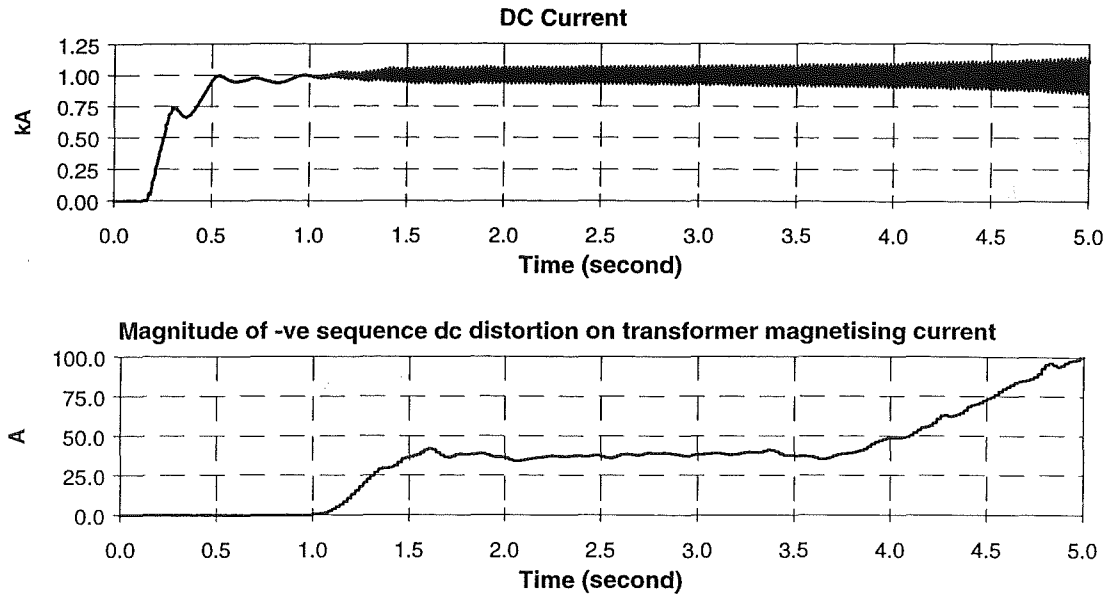


Figure E-12: Simulation results of controller D response in system 1

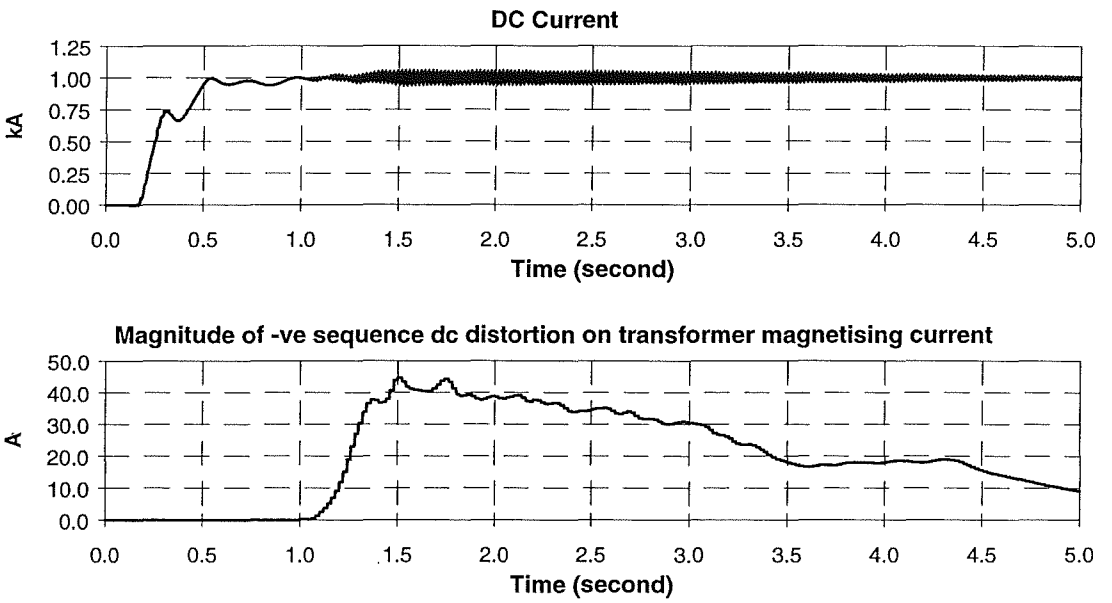


Figure E-13: Simulation results of controller D response in system 2

Finally, controller D with negative *SSF* for system 1 and positive *SSF* for system 2 exhibits opposite behaviour to controller C. This particular controller is inapplicable in system 1 as validated by the EMTDC simulation shown in Figure E-12. On the other hand, it is stable when used in system 2 as depicted in the simulation result of Figure E-13.

E.4 Conclusion

The illustrations above have highlighted the great dependencies of convertor controller behaviour towards the core saturation instability on the system impedances. Although the test systems used are very similar, the responses from some controllers can differ greatly. Furthermore, although the convertor controllers used in the demonstration are minor variants of each other and it is interesting to observe their different influence on the system susceptibility to the core saturation instability. These observations reinforce the need to undertake separate studies on different systems or on the same system under different operating conditions. The characteristics of the resultant controllers are most likely to differ under different conditions. However, the convertor controller is subjected to other requirements in addition to the prevention of this instability. Therefore, a good controller in the aspect of core saturation instability may not be appropriate or may be impractical when considered with other requirements or constraints.

Appendix F

Validation of effect of convertor parameters on Saturation Stability Factor

F.1 Introduction

In Chapter 4, the *SSF* was shown to be dependent on the convertor steady state operating parameters. The convertor steady state operating conditions are characterised by the convertor firing angle the commutation angle. From the evaluation using *SSF*, several deductions were made regarding the stability of the test system. These deductions have been validated with dynamic simulations using PSCAD/EMTDC, and the results of these simulations are described in this appendix. The test system used in the simulations is similar to that used in Chapter 3 and Appendix D, and is detailed in Appendix B.

F.2 Effect of convertor firing angle

When a convertor is operating in the rectification mode, the system *SSF* and hence stability was found to be inversely proportional to the firing angle. Table F-1 shows the three cases used to demonstrate the effect of convertor firing angle on the system stability. Only changes to the firing angle are considered in this illustration as the dc current is adjusted in each case so as to achieve the same commutation angle.

Test case	**1**	**2**	**3**
Firing angle	20°	22°	18°
SSF	-0.11	-0.29	0.09

Table F-1: Test cases for validation of the effect of convertor firing angle on *SSF*

With firing angle of 20° in test case 1, the *SSF* is negative at -0.11 indicating instability. This is confirmed by the simulation results shown in Figure F-1. Moreover, the small value suggests that the instability will grow slowly which is again depicted by the slow growth in the dc current distortion and in the level of saturating dc current. However, as the instability develops, the transformer becomes more saturated which will accelerate the build up of the distortions. This accelerating effect is demonstrated by the large increase in the distortion levels after the time of 4 seconds.

A slight increase in the firing angle to 22°, as in case 2, lowers the *SSF* to -0.29. A more negative *SSF* implies that the instability will build up at a faster rate. Figure F-2 shows the simulation results of case 2 and the presence of this type of instability is clearly evidenced in the figure. Moreover, a faster build up of the saturating dc current level in the transformer

magnetising current and the distortions in the dc current is also observed confirming the deduction of a more negative *SSF*. A substantial amount of distortion is observed at the time of 3 seconds compared to case 1.

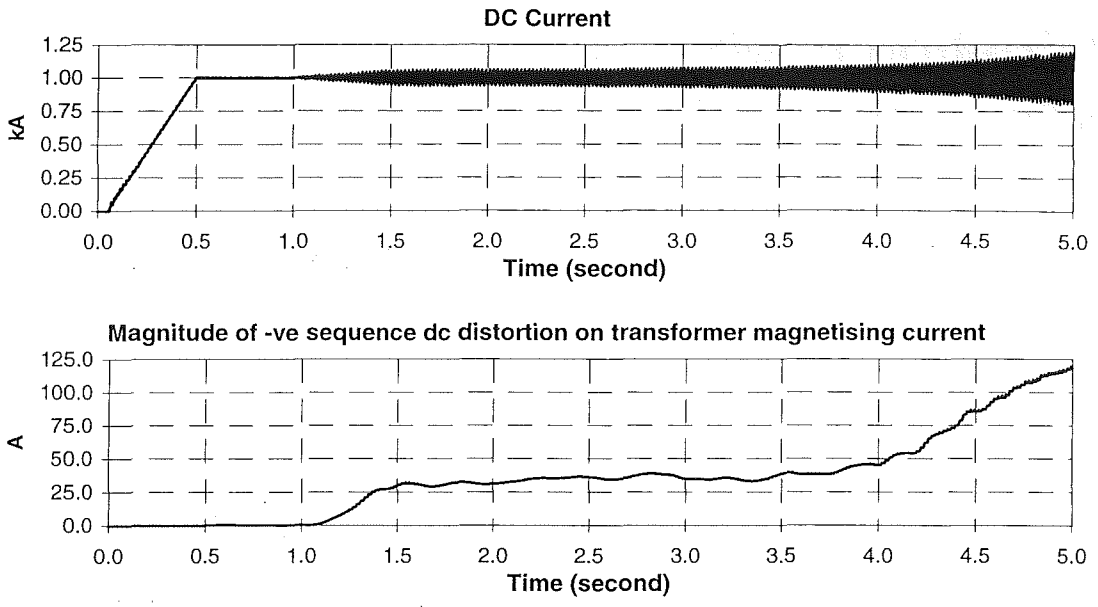


Figure F-1: Simulation results of case 1 for validation of the effect of firing angle

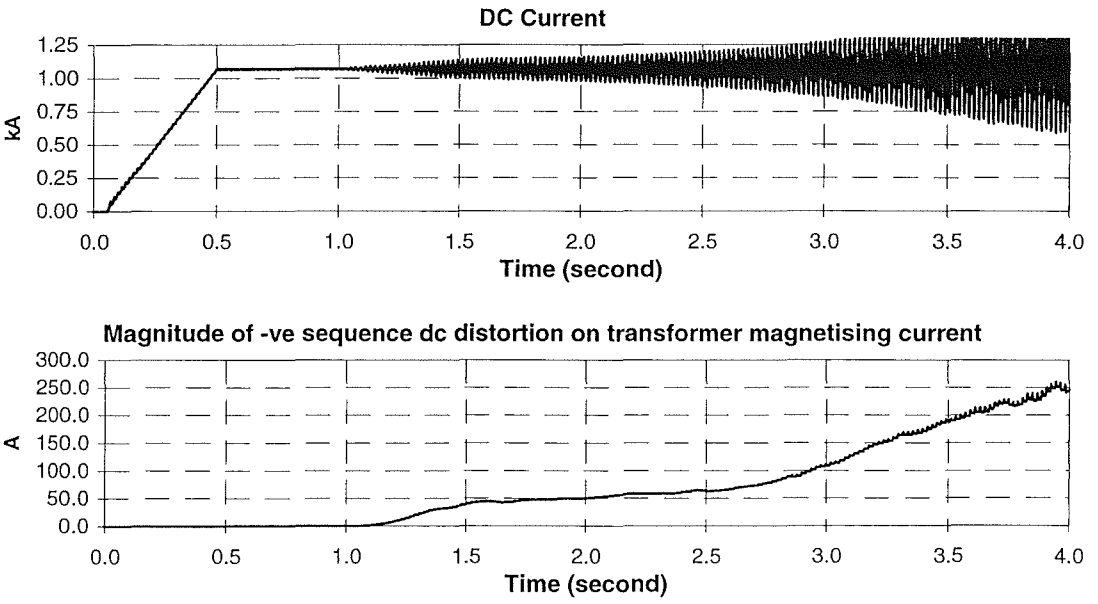


Figure F-2: Simulation results of case 2 for validation of the effect of firing angle

In case 3, the firing angle is reduced to 18° making the *SSF* positive at 0.09. Although the positive *SSF* implies that the system will become stable, its low value indicates that the level of damping is low and hence it will take a long time for the distortion to decay away. Figure F-3 shows the results of the simulation for case 3. Although the transformer is subjected to similar level of saturation as that in case 1 and 2, the distortions decay away after the external

disturbing signal is removed. Moreover, the level of saturating dc current decreases slowly confirming the low rate of decay predicted from the low *SSF* value. At the time of 5 seconds, there is still a small level of saturation on the transformer, but the distortion on the dc current has somewhat disappeared.

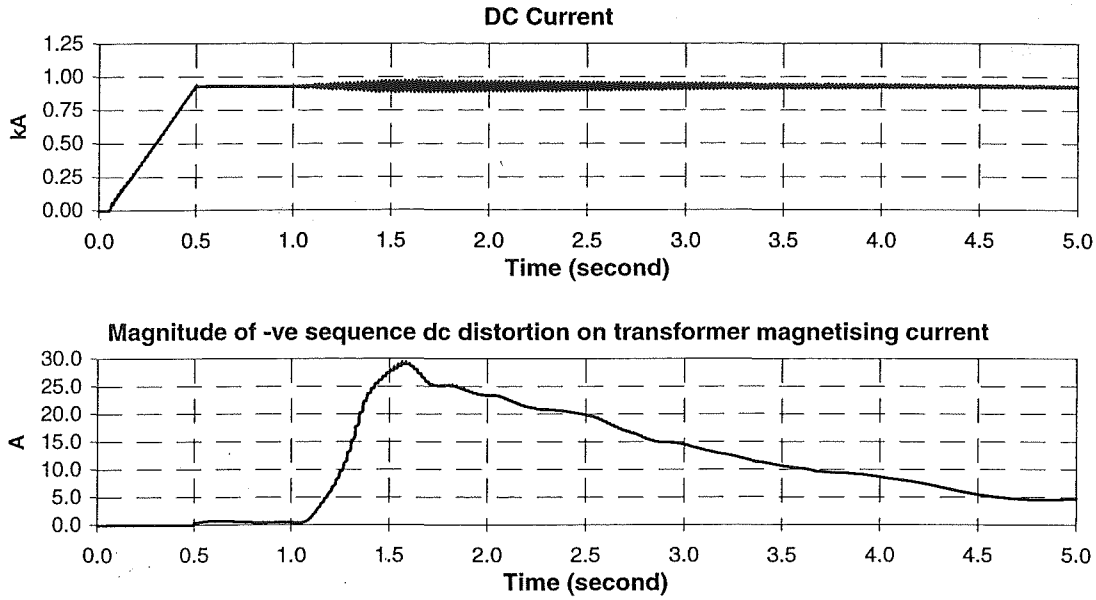


Figure F-3: Simulation results of case 3 for validation of the effect of firing angle

The above dynamic simulations have validated the predictions made from the *SSF* approach that the system stability is inversely proportional to the convertor firing angle. A system operating at high firing angle is more likely to develop core saturation instability than that operating at low firing angle, even under similar operating conditions with similar commutation angles. However, changes to the firing angle will usually affect the commutation period which in turn affects the system stability. Therefore, the influence from the convertor firing angle will be more substantial if the variation in commutation angle is also taken into account.

F.3 Effect of convertor commutation angle

The convertor commutation process is known to introduce an apparent damping on the convertor dc side which assists in stabilising the system. The level of this apparent damping is directly proportional to the length of the commutation period. Therefore, the system stability as indicated by the *SSF* was shown to be directly proportional to the commutation period. Table F-2 shows the test cases used to validate these deductions. The length of the commutation period was varied by altering the commutating reactance which is taken as the transformer leakage reactance.

Case 1 has a leakage reactance of 0.13 pu resulting in a commutation period of 0.214 radian and the *SSF* was evaluated to be negative at -0.11. This prediction of instability is confirmed by the EMTDC simulation result of Figure F-4.

Test case	1	2	3
Commutating reactance X_c (pu)	0.13	0.06	0.20
Commutation angle (Radian)	0.214	0.111	0.303
SSF	-0.11	-0.93	0.46

Table F-2: Test cases for validation of the effect of commutation angle on *SSF*

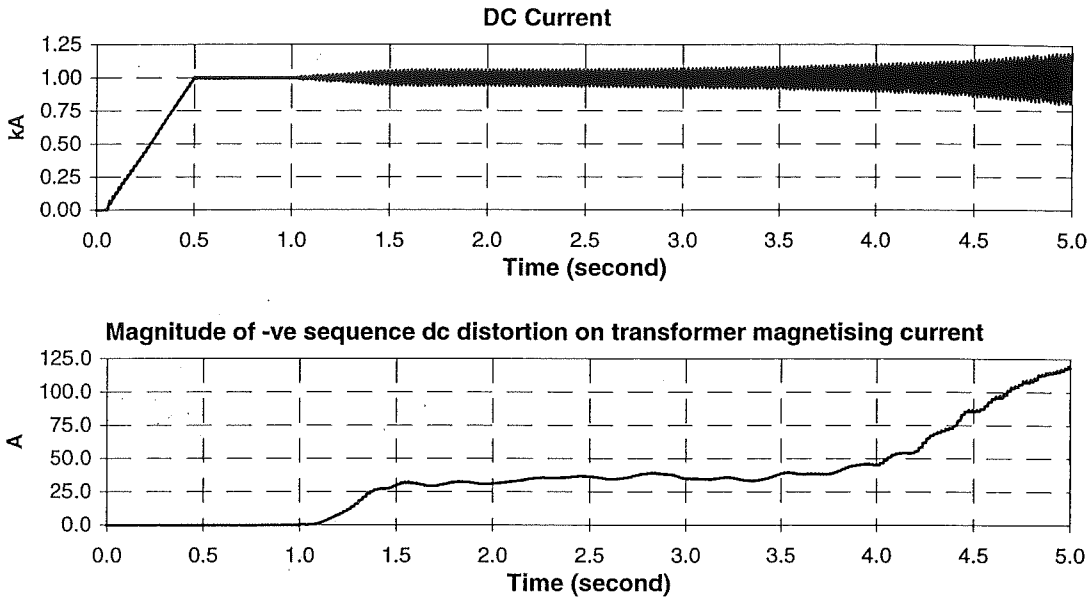


Figure F-4: Simulation results of case 1 for validation of the effect of commutation angle

In test case 2, the transformer leakage reactance is reduced to 0.06 pu dropping the commutation period down to 0.111 radian. The *SSF* also decreases accordingly to -0.93 suggesting that the build up of the core saturation instability will be faster in this case as compared with case 1. This deduction is validated by the simulation result shown in Figure F-5. It took about 2 seconds for the saturating dc current to reach 100 A in case 2 while in case 1, it took more than 3 seconds.

In case 3, the transformer leakage reactance is raised to 0.20 pu causing the *SSF* to become positive at 0.46. This indication of stability is confirmed by the dynamic simulation results shown in Figure F-6. As soon as the disturbing firing angle modulation is removed at the time of 1.5 seconds, the distortions in the system quickly die away to negligible levels.

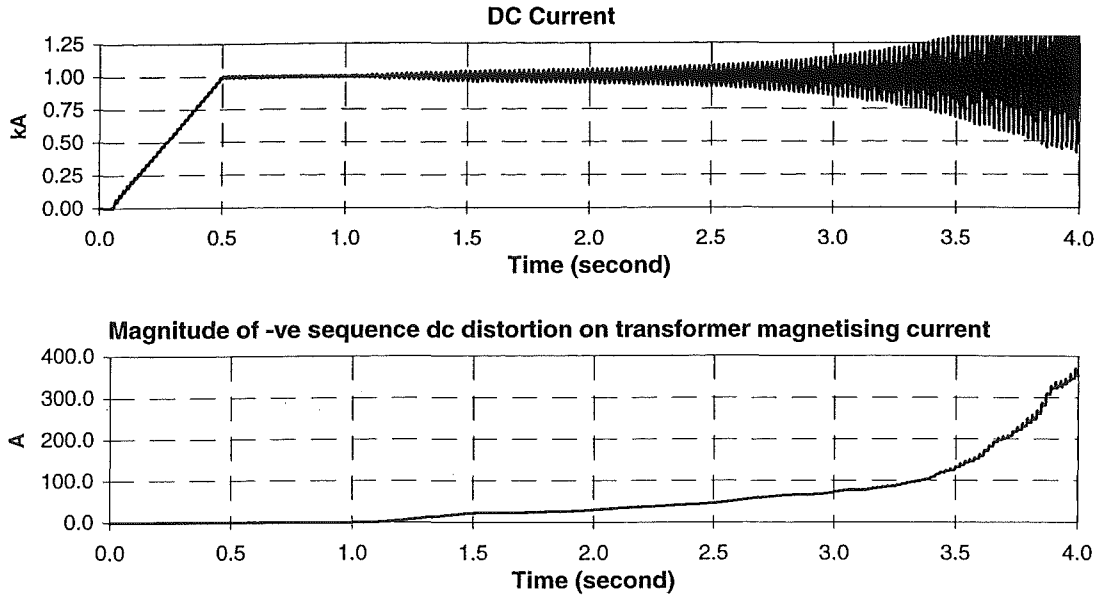


Figure F-5: Simulation results of case 2 for validation of the effect of commutation angle

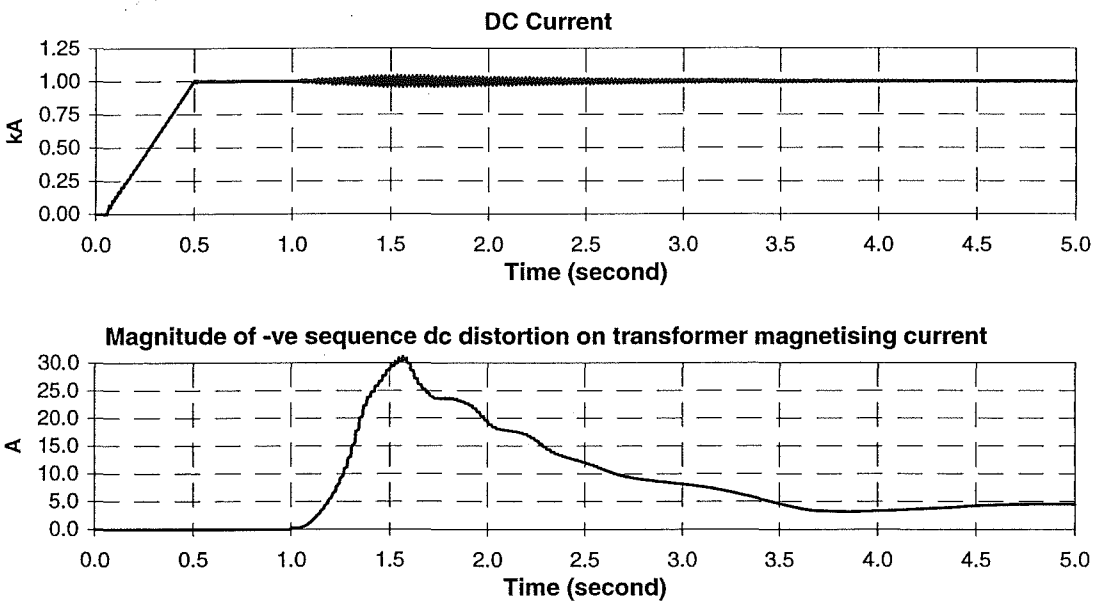


Figure F-6: Simulation results of case 3 for validation of the effect of commutation angle

F.4 Conclusion

The simulation described in this appendix have validated the predictions made from the evaluation of *SSF* that HVDC system (rectifier) operated at large firing angle and with short commutation period is more susceptible to the core saturation instability compared to one operated at low firing angle and with long commutation period. Although all of the simulations were carried with the convertor operating in rectification mode, sufficient agreements were obtained to instill further confidence in the *SSF* approach. In the inversion

mode, the system is more susceptible when the firing angle is low which corresponds to short commutation period.

Appendix G

Accepted publications

1. Chen, S., Wood, A.R. and Arrillaga, J., "***HVDC Convertor Transformer Core Saturation Instability - A Frequency Domain Analysis***", Accepted for publication in the IEE Proceedings - Generations; Transmission; Distribution, December 1995.
2. Chen, S., Wood, A.R. and Arrillaga, J., "***A Direct Frequency Domain Investigation of the Properties of Convertor Transformer Core Saturation Instability***", Accepted for presentation at the IEE Sixth International Conference on AC and DC Transmission at London, United Kingdom, 30th April - 3rd May 1996.